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# MS-7850 ATX Ver: 11

Intel -ShakeBay plamform

CPU:

INTEL-Haswell LGA1150

CPU DISPLAY

HDMI(portB) DVI (port C)

System Chipset:

INTEL-LYNX

OnBoard Chipset:

HD Audio Codec:ALC887 Co-lay 892

LAN-RTL8111G Co-lay 8106G

SIO:Nuvoton NCT6779

Main Memory:

DDRIII (1066/1333/1600MHz) \* 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot \* 1

PCI Express (X1) Slot \* 2

PCI Slot \* 2

PWM:

VRD12 - ISL95812( 3 Phase 12MOS , Power pak)

Other:

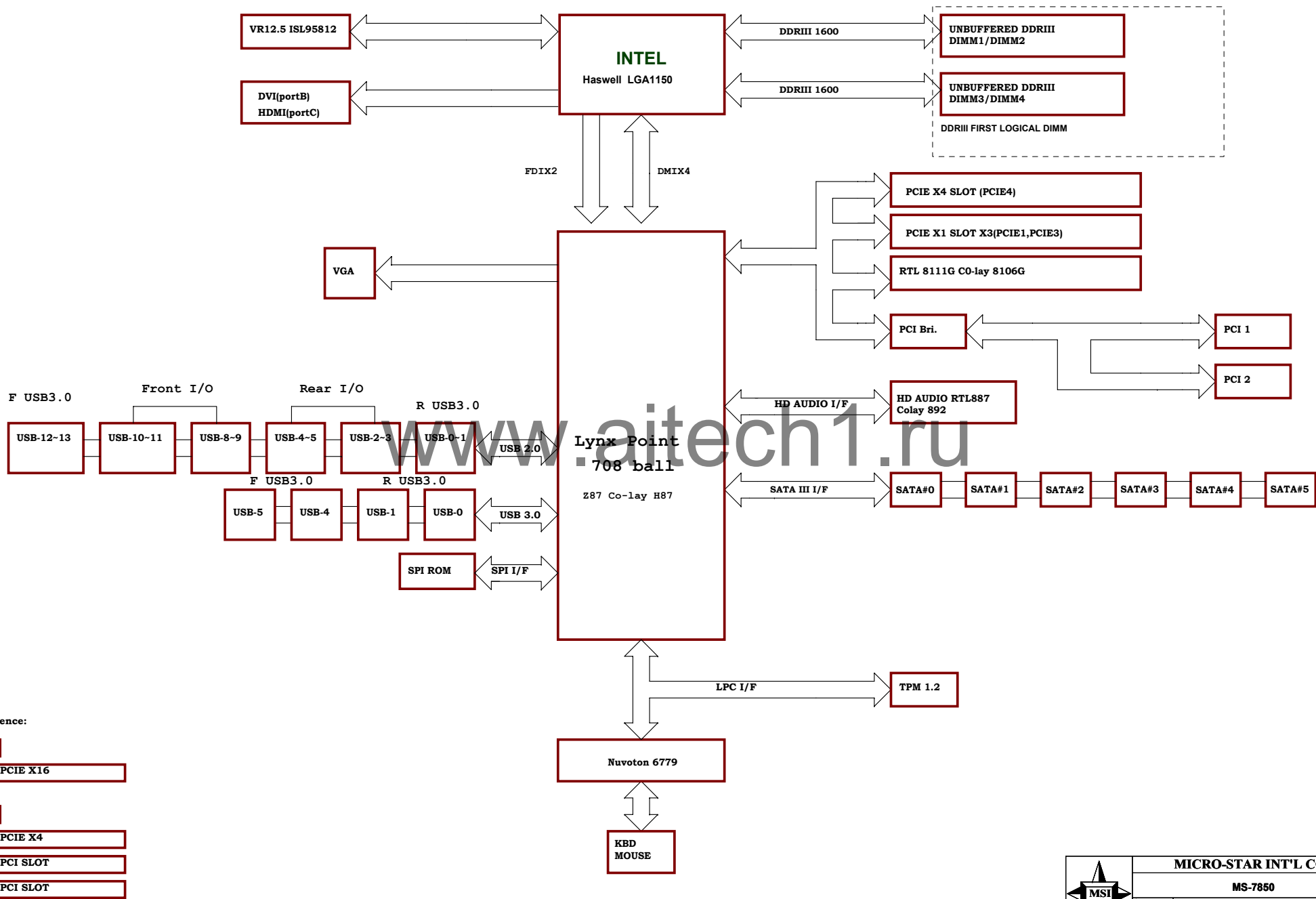
SATA(SATA3-500MB/s) \*6

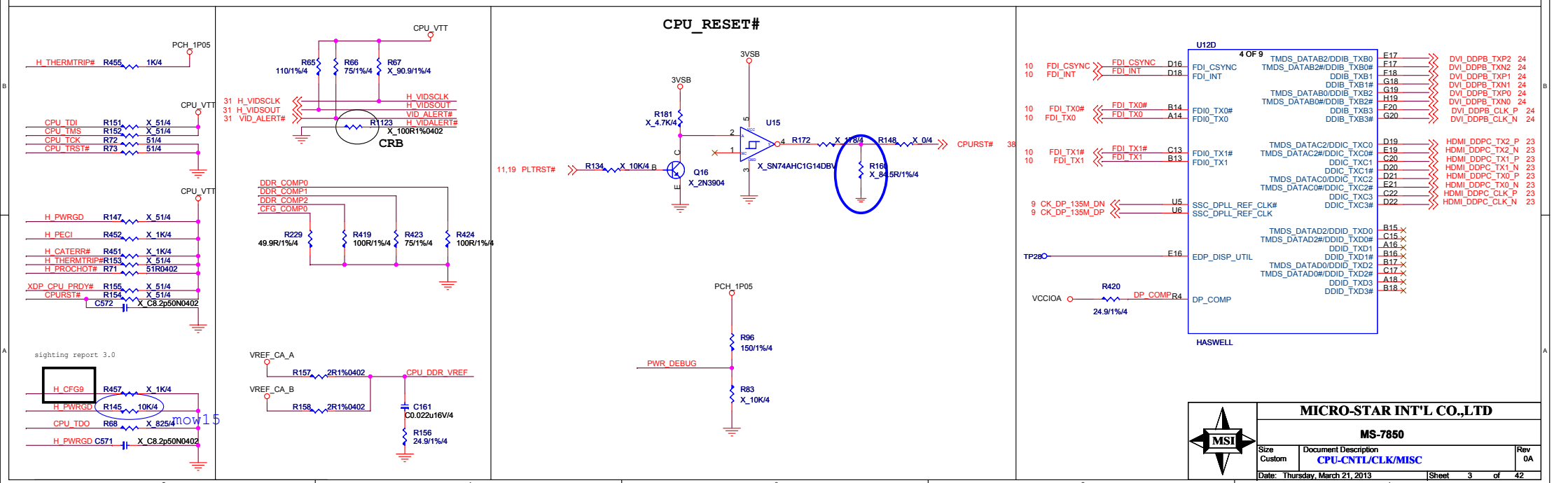
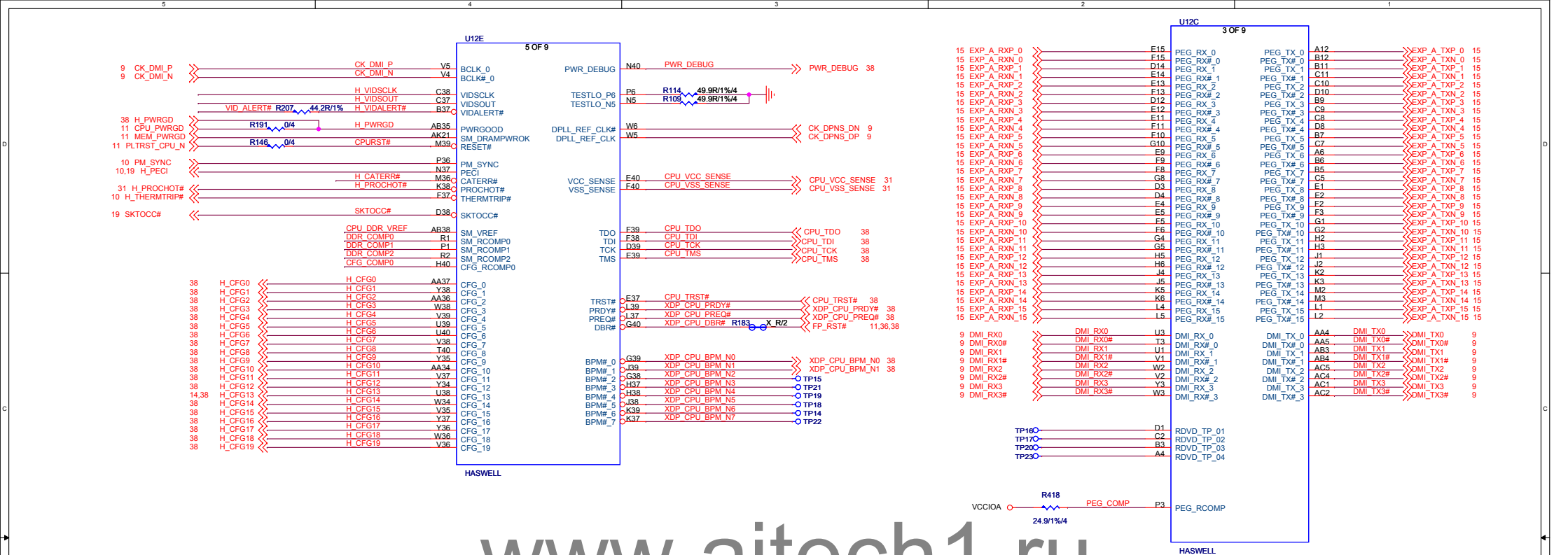
REAL USB2.0 \*4

FRONT USB2.0 \*4

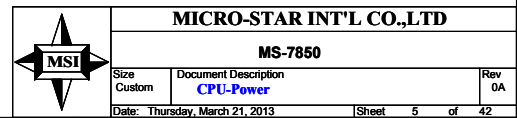
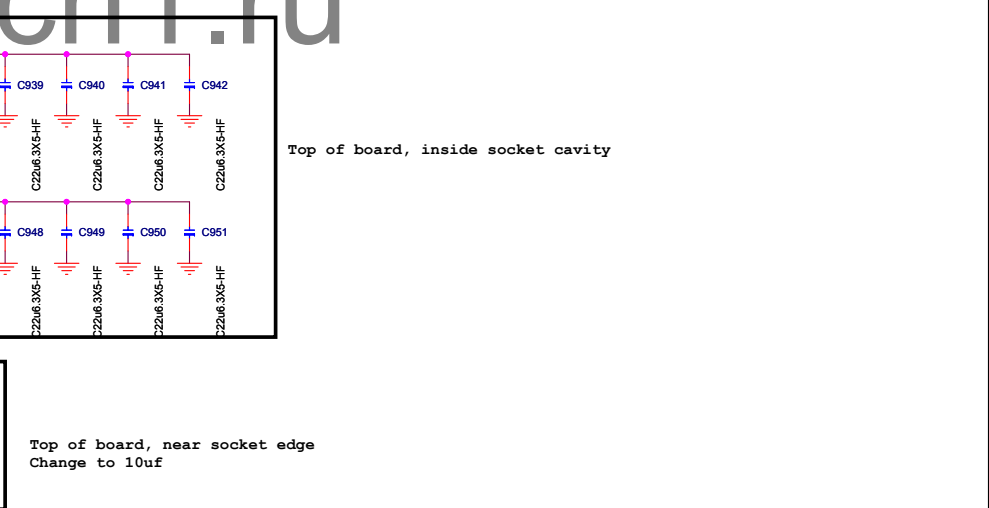
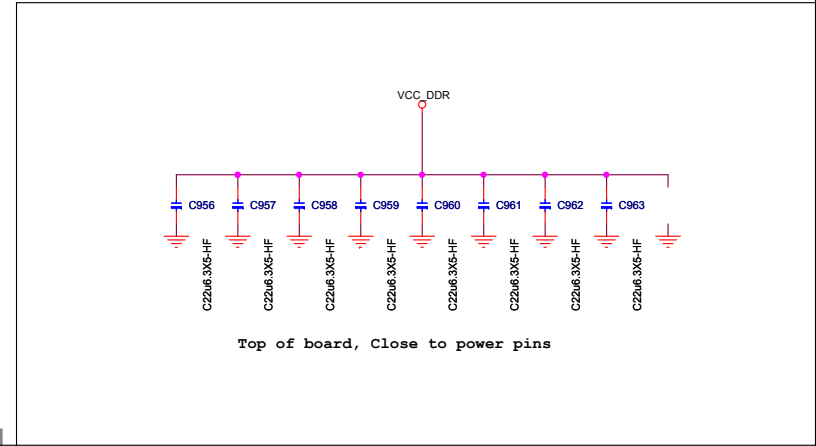
REAL USB3.0 \*2

FRONT USB3.0 \*2





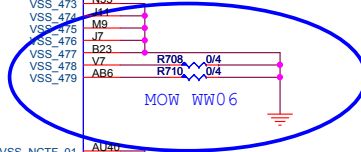




GND

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GND



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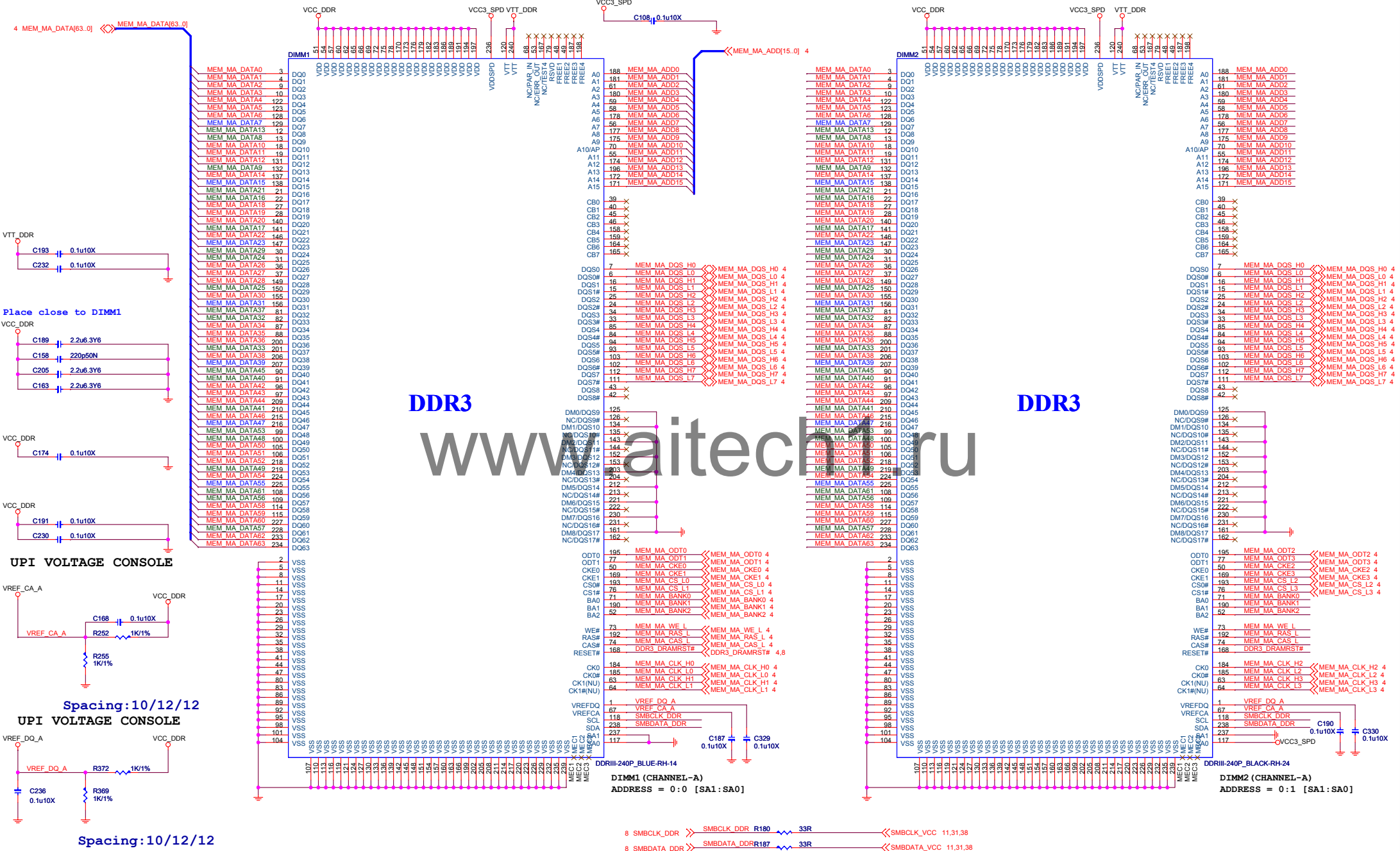
MS-7850

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Custom	CPU-GND	0A
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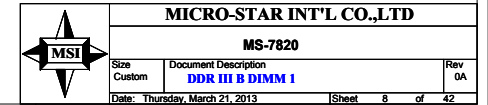


# DDRIII DIMM\_A0

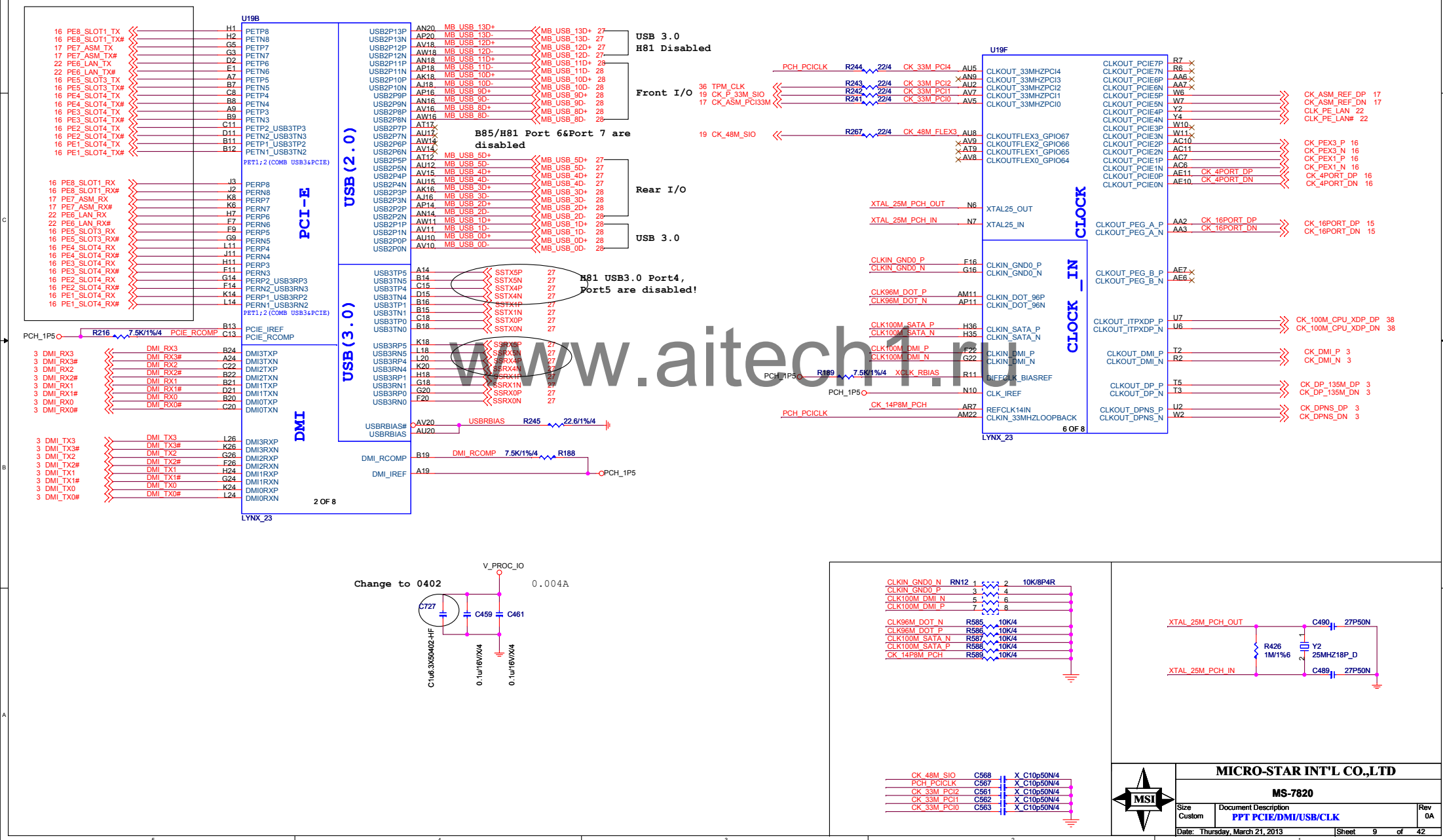
# DDRIII DIMM\_A1



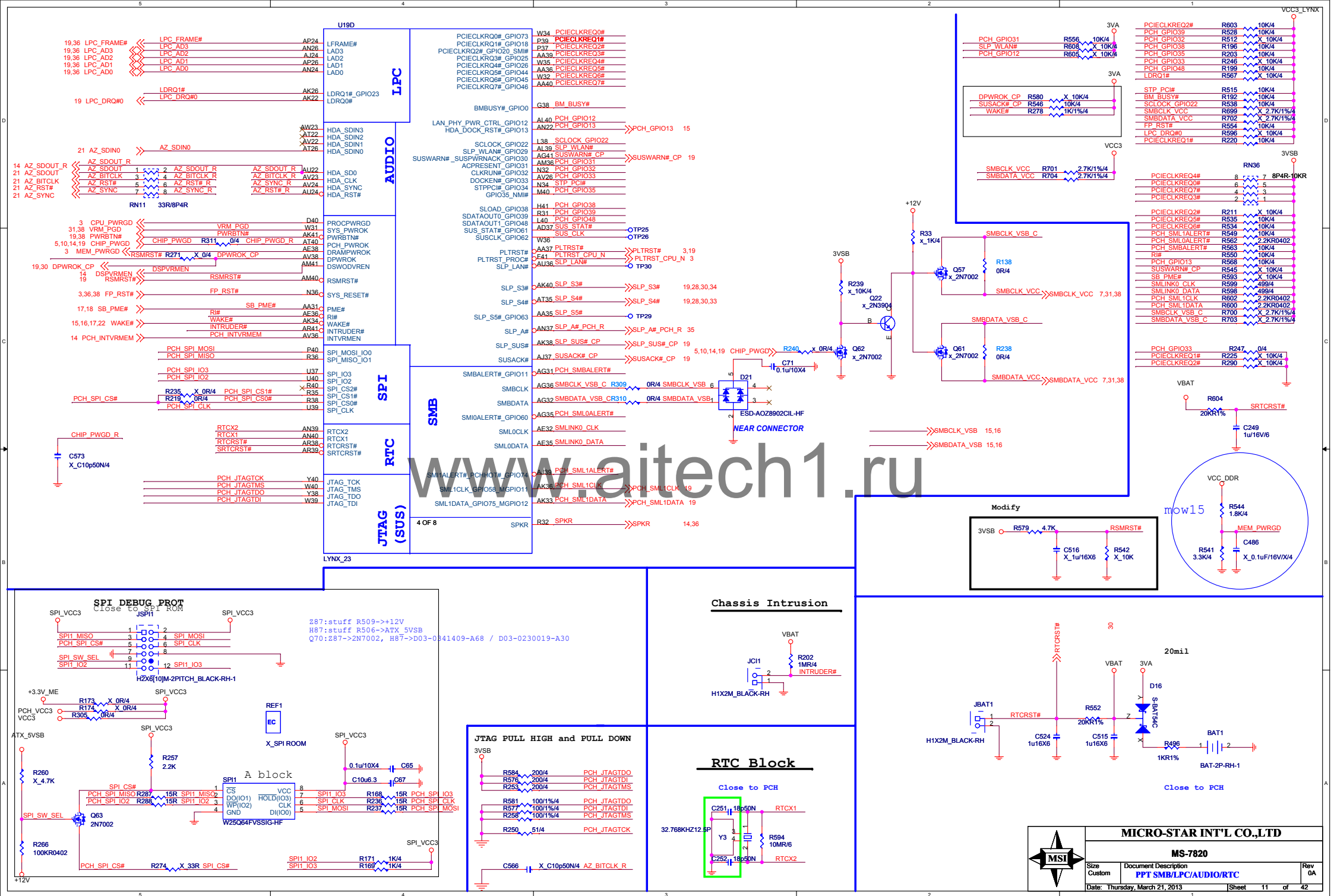
## DDRIII DIMM\_B1



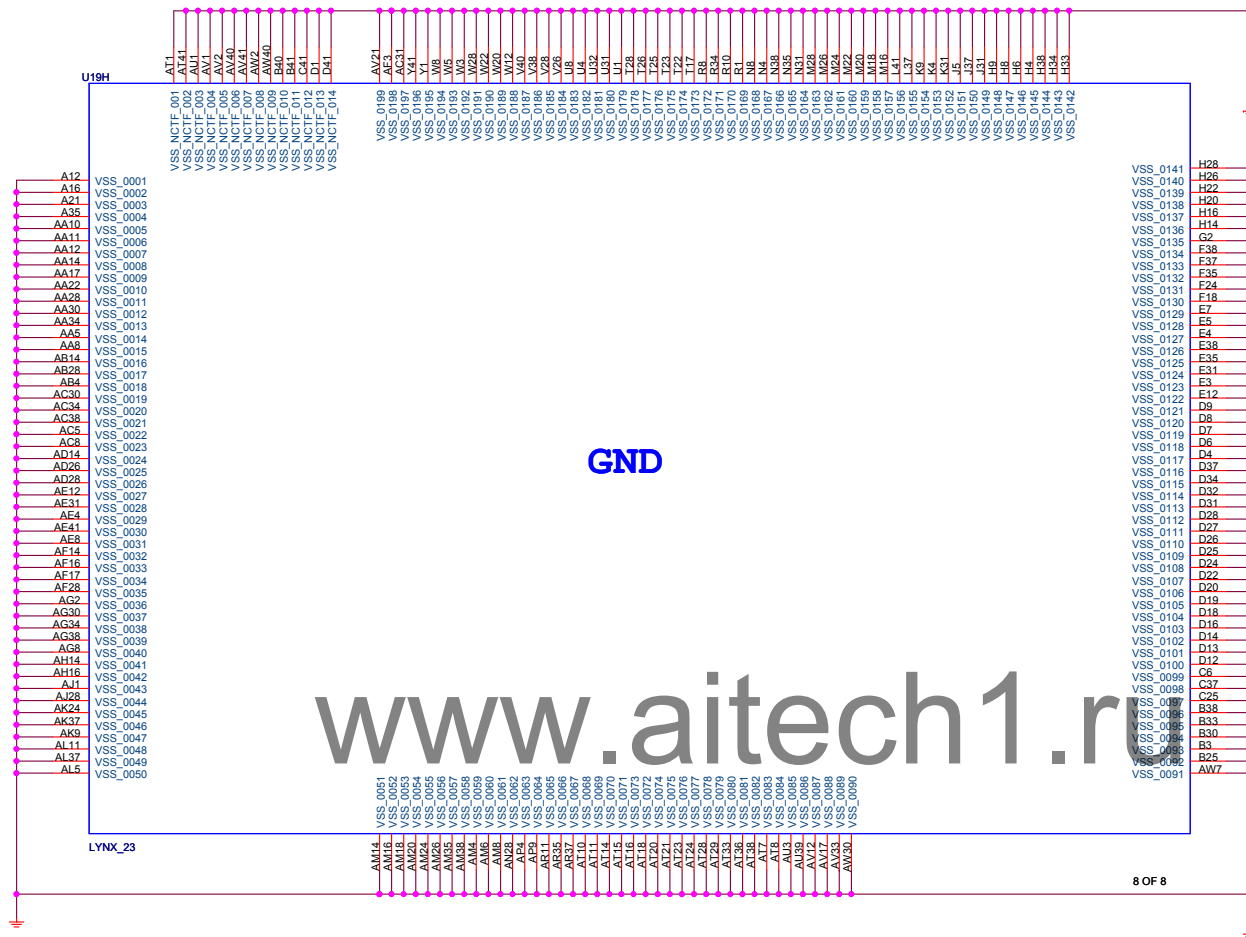












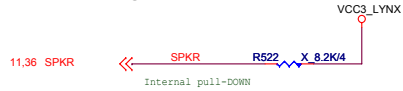
Pull high to enable integrated VRM



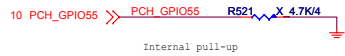
Pull high to enable integrated Deep-Sx well On-die VR



Internal weak pull down  
Pull high to enable "No Reboot" mode

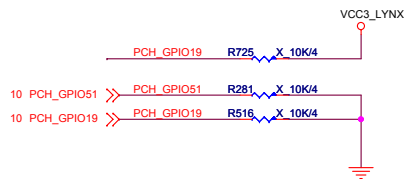


Internal weak pull up  
Pull low to enable "Top-Block Swap" mode



BOOT DEVICE	GPIO51	GPIO19
LPC	0	0
SPI	1	1

Default



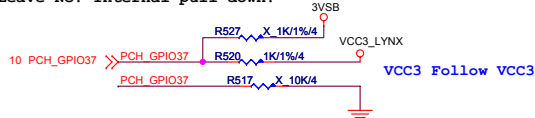
Do not pull low.  
Connect to ground with 1k Ohm pull-down resistor.



Enable TLS:

Pull up with 1k Ohm to VccSus3.3.  
Default (Disable TLS):

Leave NC. Internal pull down.

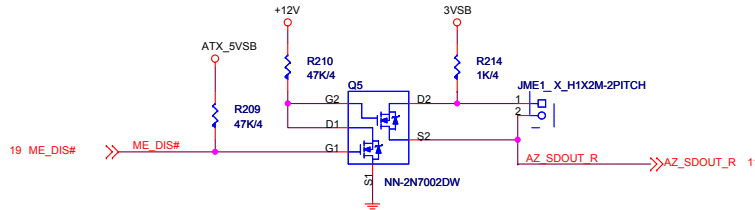


Default:

Do not pull high.

Disable ME in Manufacturing Mode:

Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.



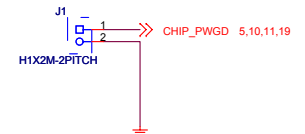
Internal weak pull down (function reserved)  
Signal should not be pulled high when strap is sampled



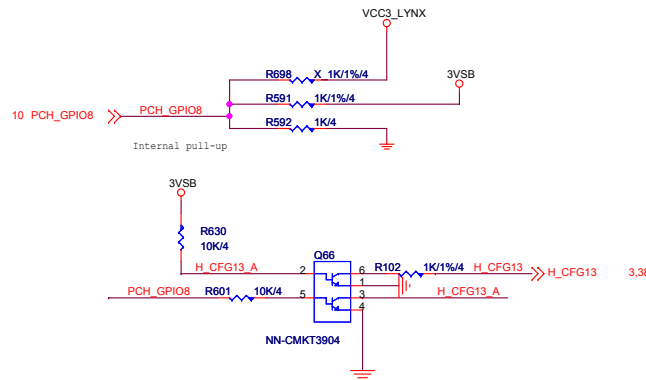
PCIE1 and SATA4 flexible IO function select  
High: SATA Low: PCIE



For test cpu voltage



Follow CRG 1.0

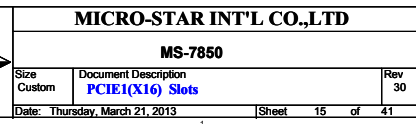
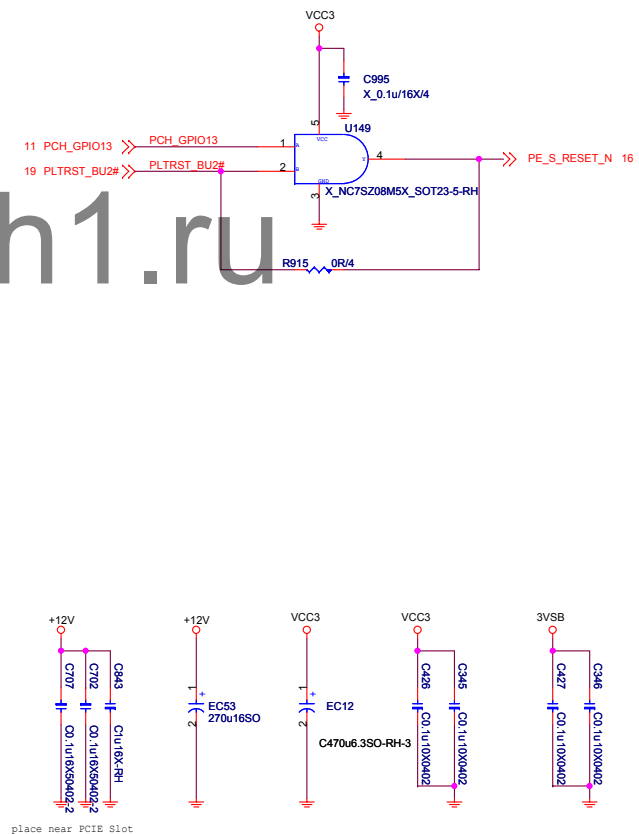


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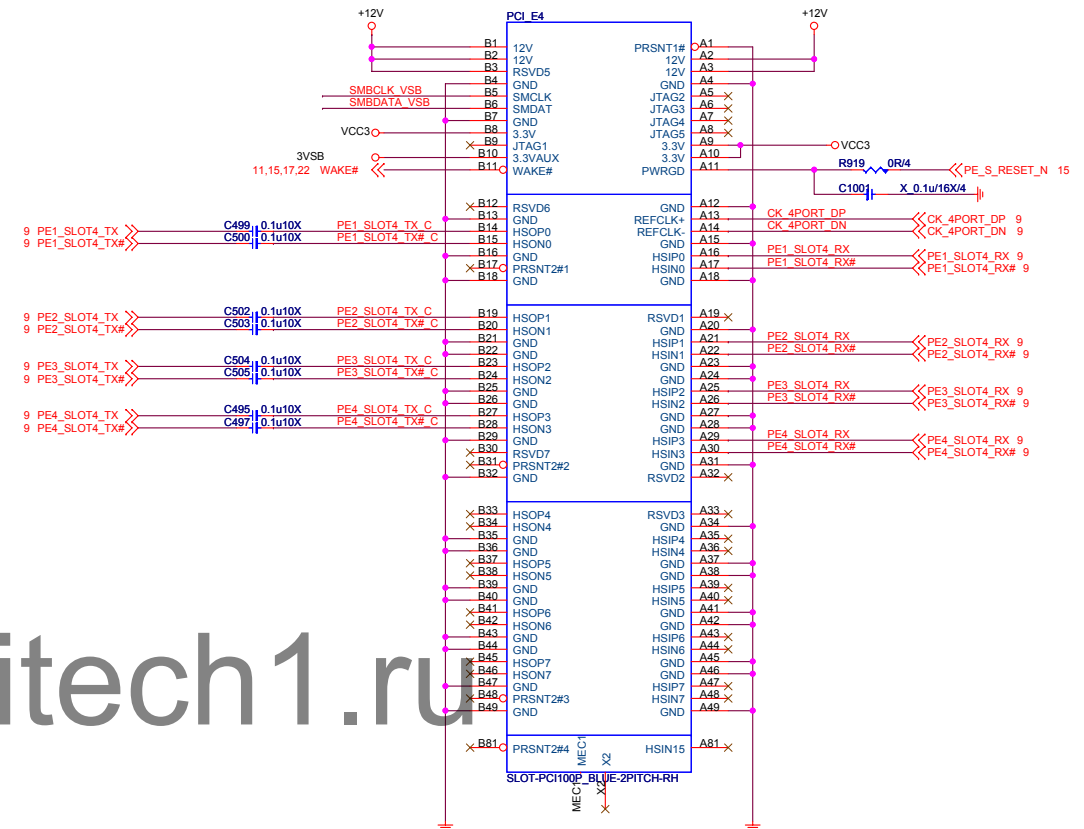
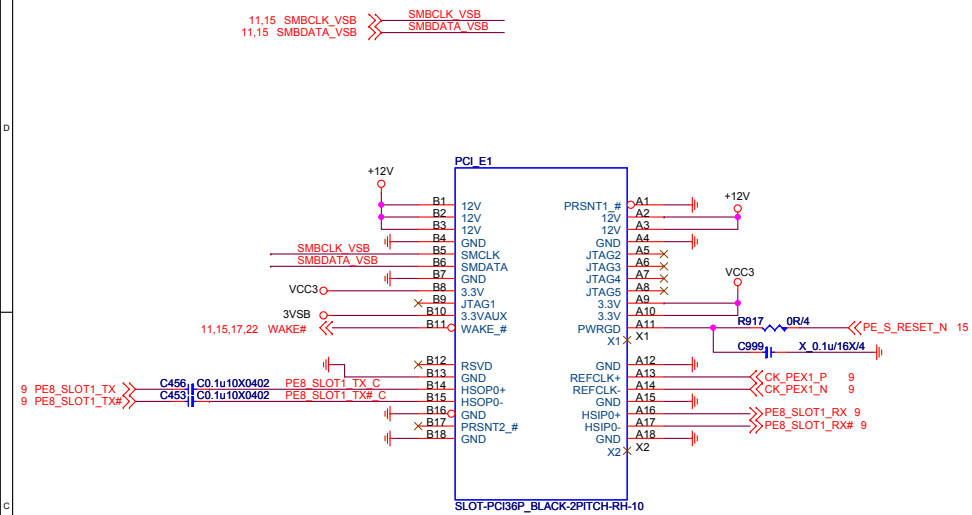
MS-7820

Size Custom	Document Description PPT STRAPS	Rev 0A
Date: Thursday, March 21, 2013	Sheet 14 of 42	

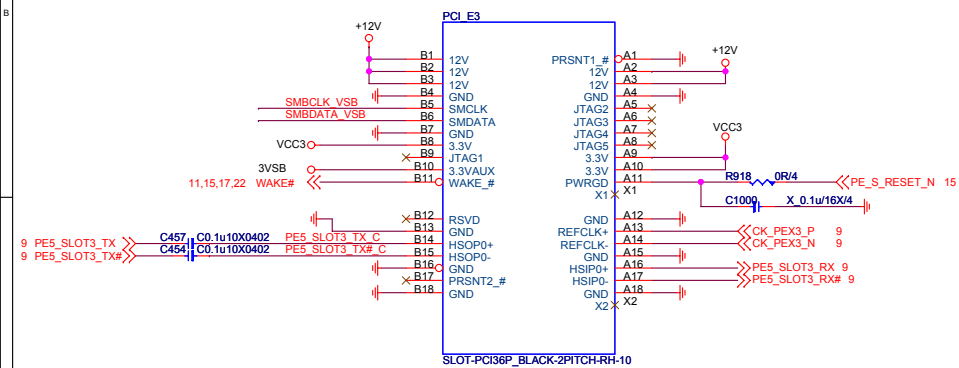




PCI Express X4 Slot



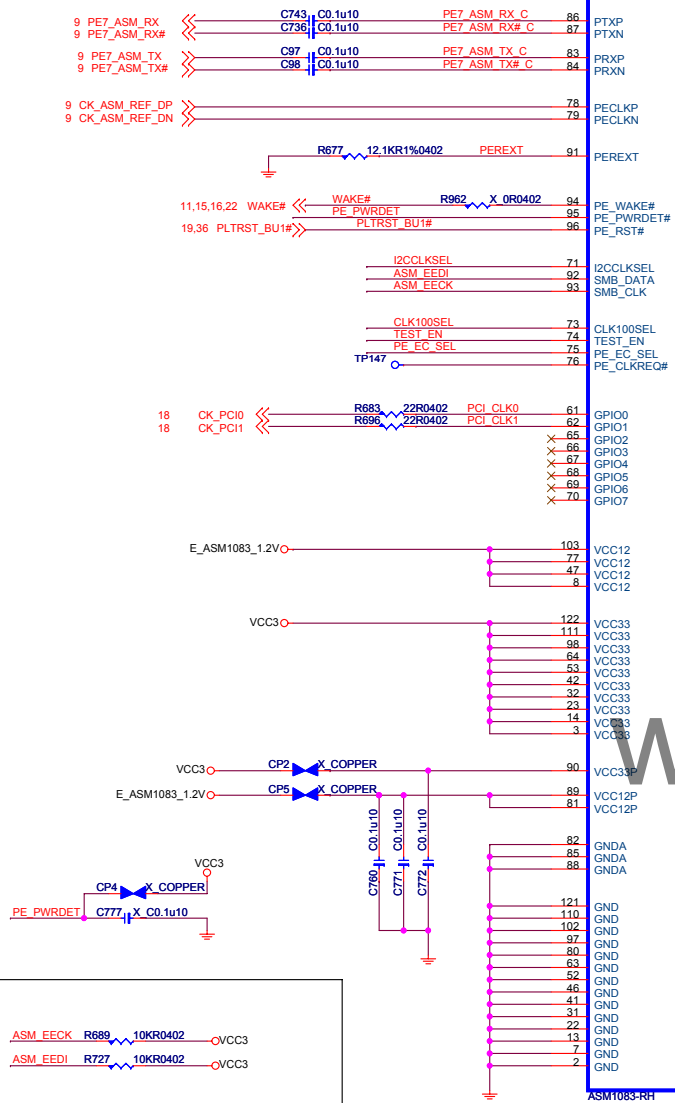
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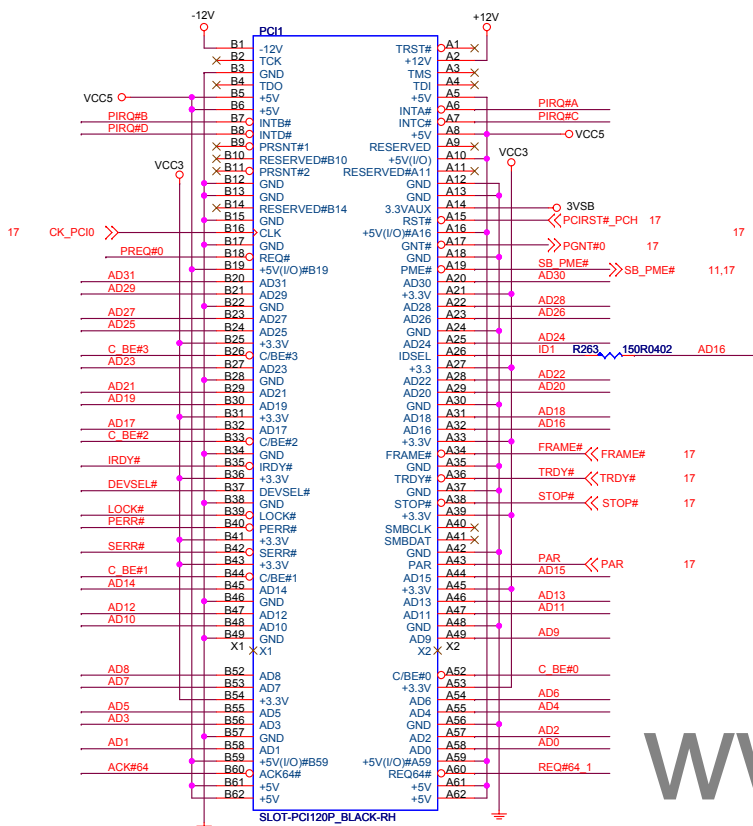


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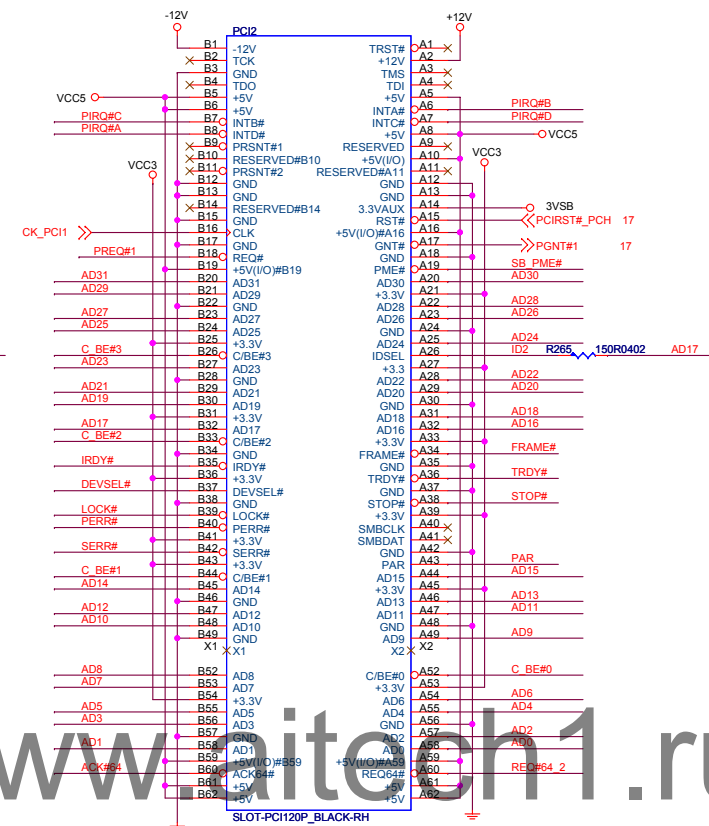
MS-7850

Size Custom	Document Description <b>PCIE3(X1) &amp; PCIE4(X4.) Slots</b>	Rev 0A
Date: Thursday, March 21, 2013		Sheet 16 of 44



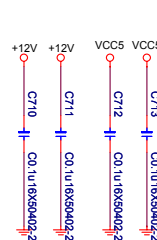
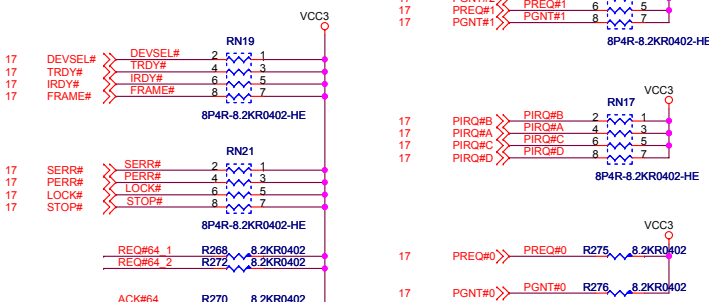
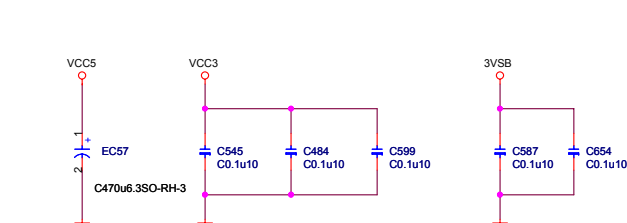


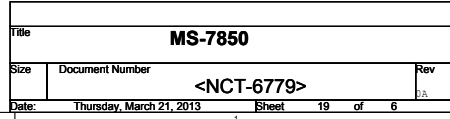
**IDSEL = AD16**  
**MASTER = PREQ#0**  
**PIRQ#A**



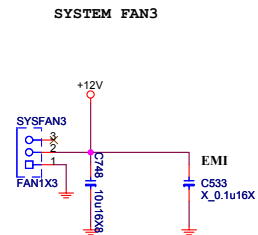
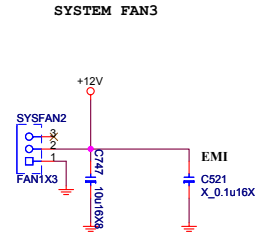
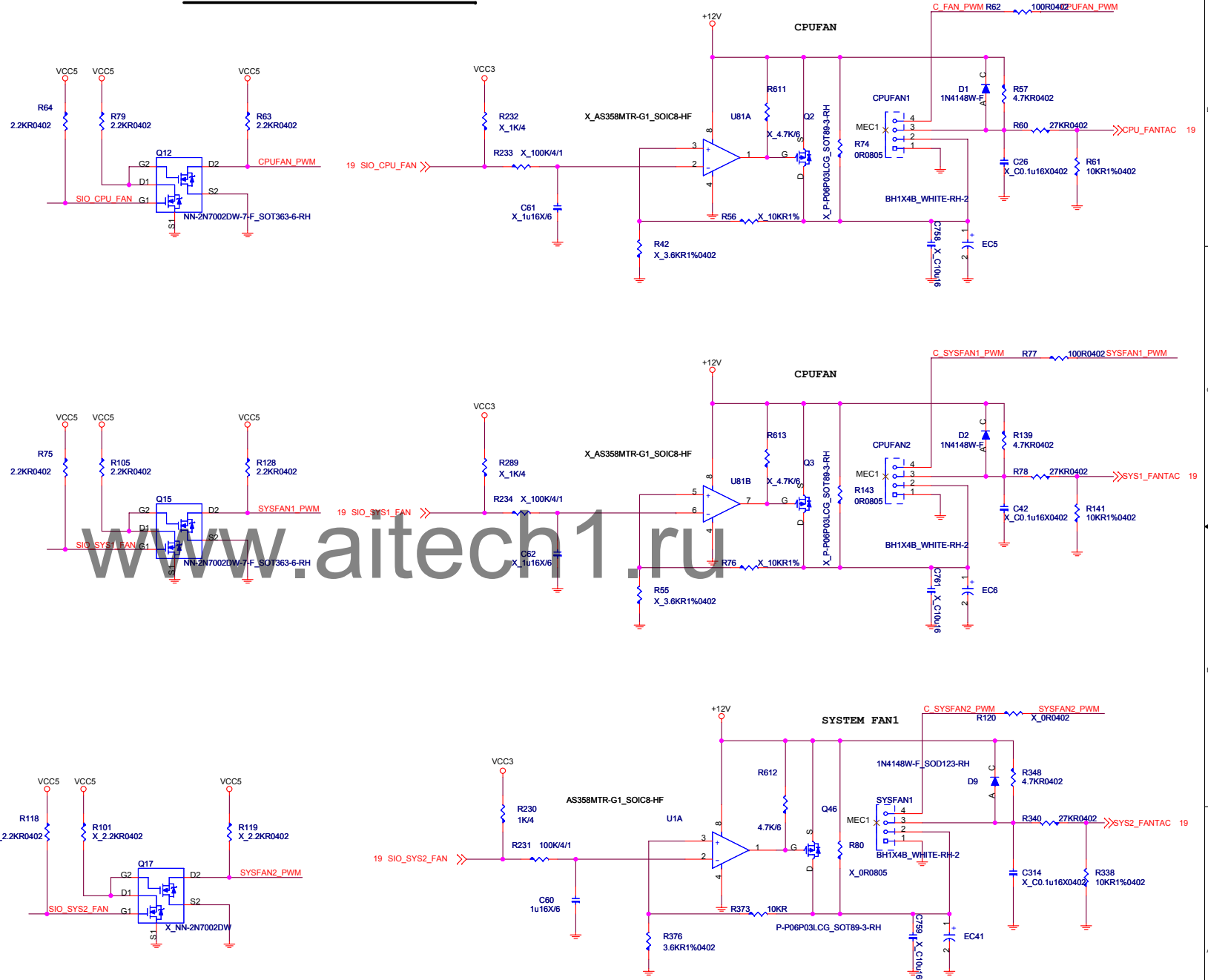
**IDSEL = AD17**  
**MASTER = PREQ#1**  
**PIRQ#B**

### PCI PULL-UP / DOWN RESISTORS





# FAN-COUNTROL CIRCUIT



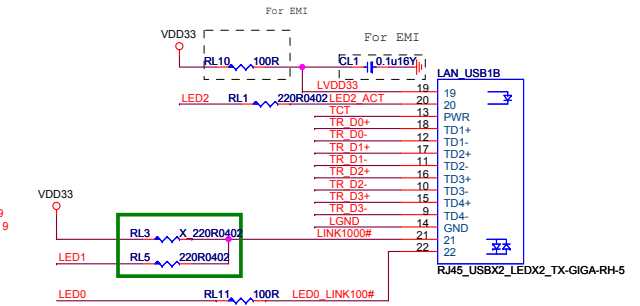
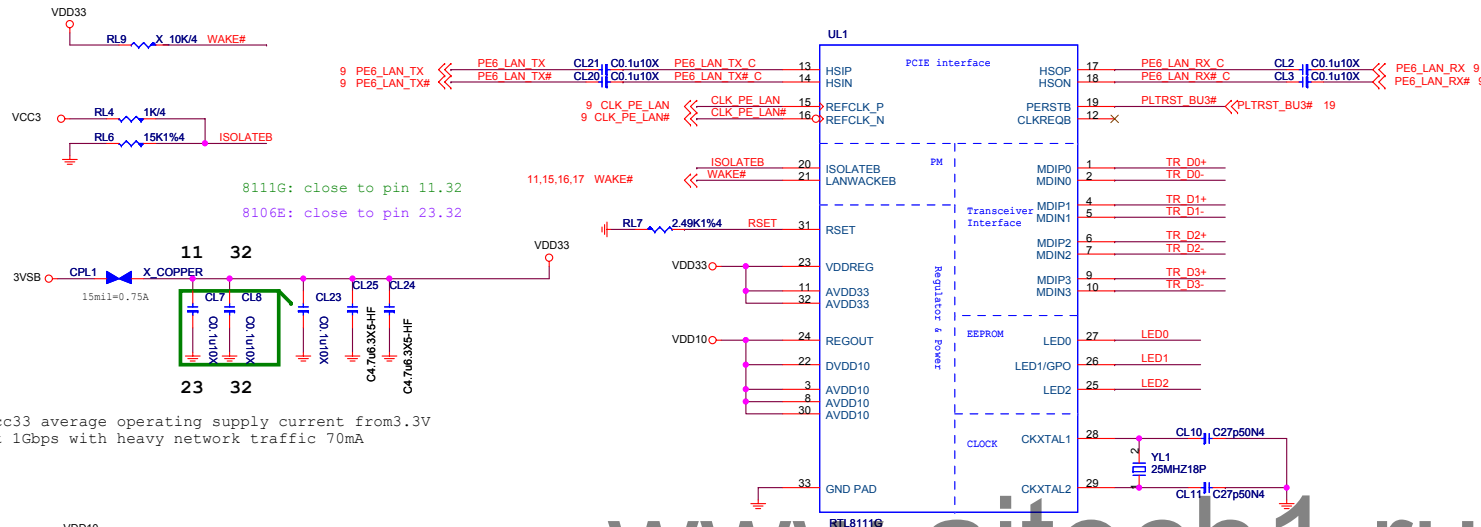


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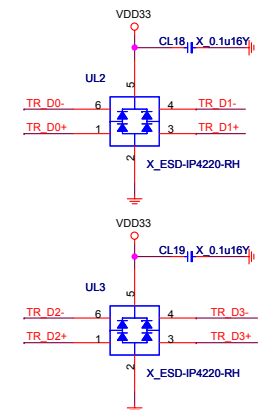
# RTL8111G Giga LAN

## RTL8106E 10/100M LAN

### LAN Connector



### Reserve ESD Protect

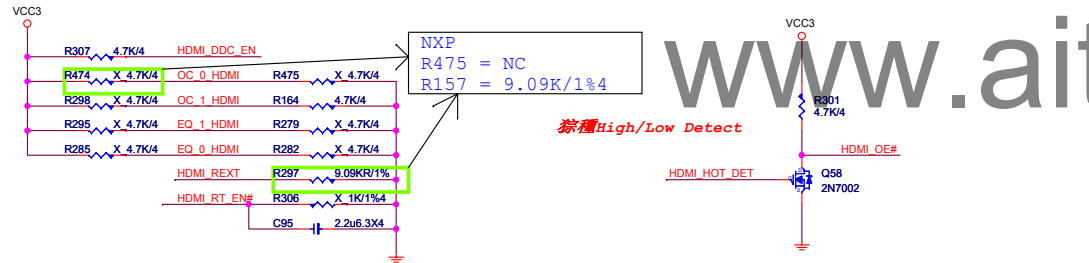
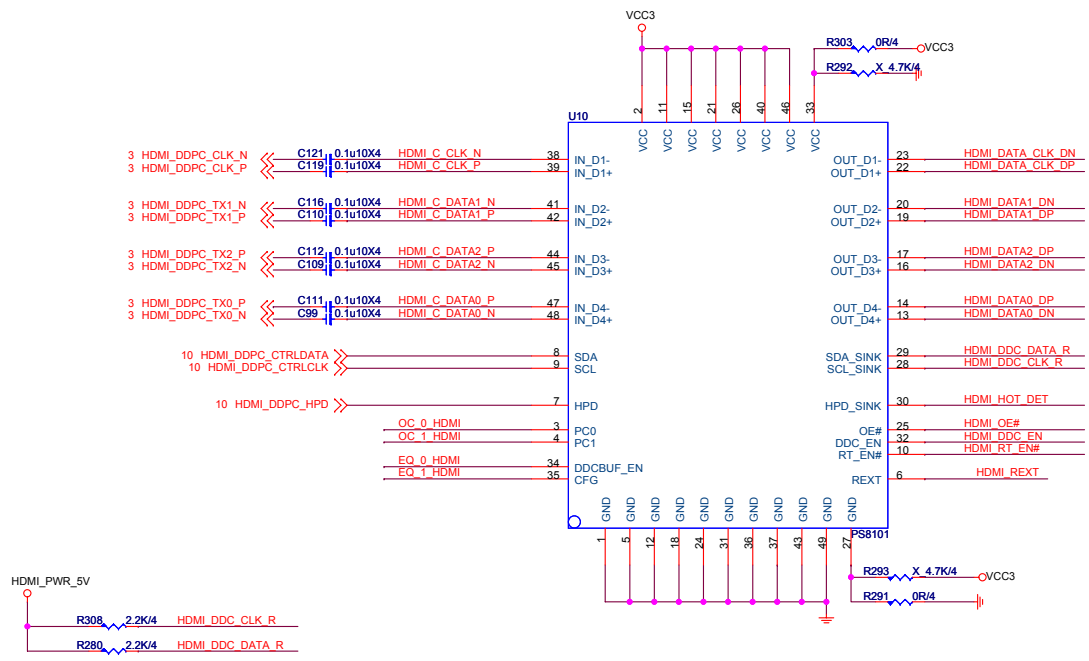


	MICRO-STAR INT'L CO.,LTD		
	MS-7850		
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HDMI level shifter

Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

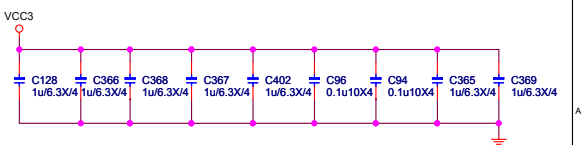
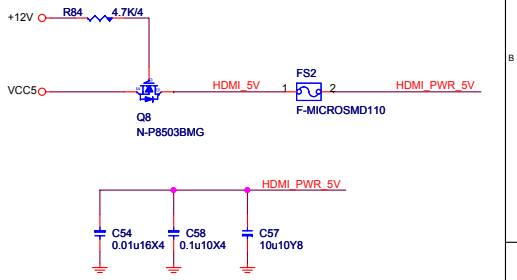
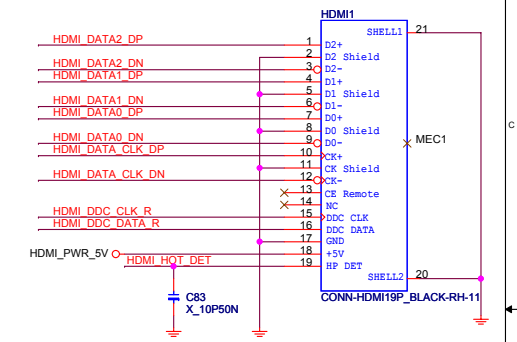
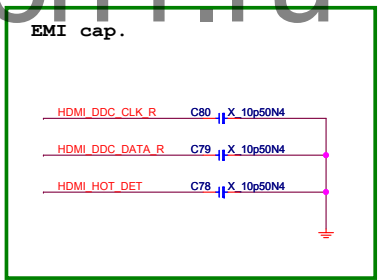
Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMI_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMI_CTRL_DATA	



	"0"	"1"
DDC_EN	DDC level shifter disable	DDC level shifter enable
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances
OE#	enable	the chip is power down and input termination resistors will be at high impedance.
HPD_SINK	disable	enable
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.	
REXT		

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	



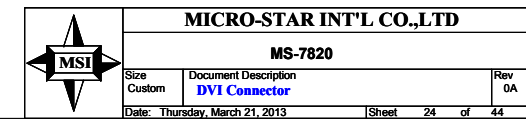
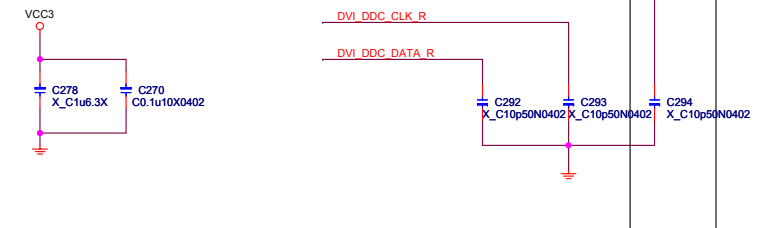
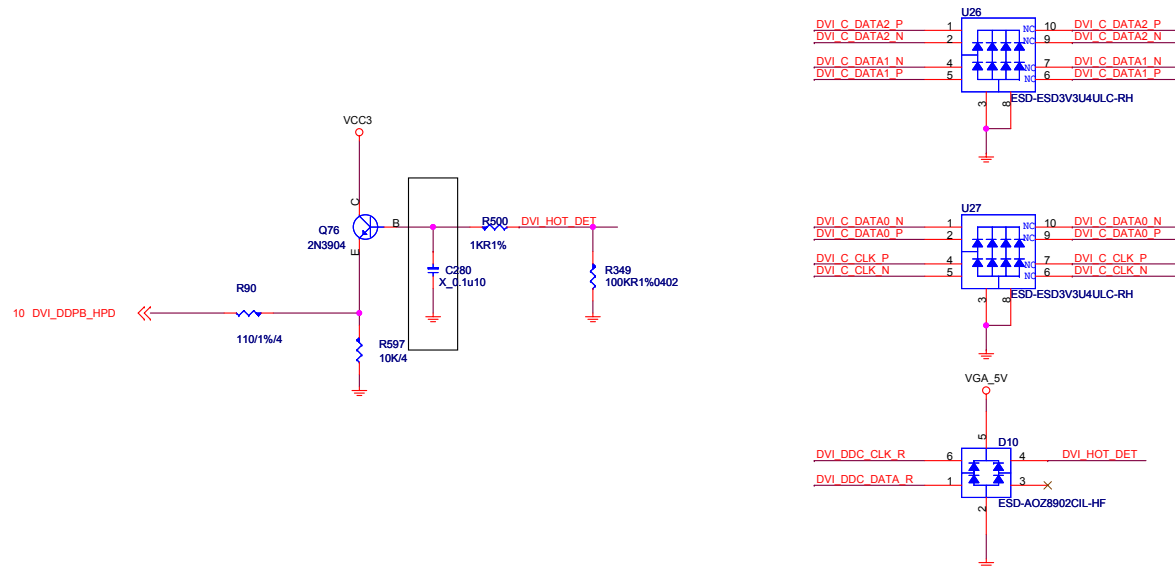
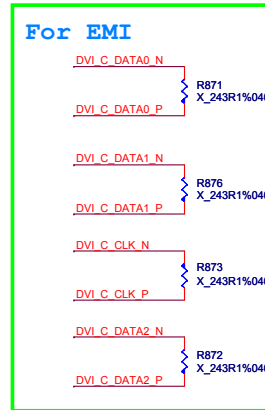
**MICRO-STAR INT'L CO.,LTD**

**MS-7851**

Size Custom Document Description **HDMI Connector** Rev 0A

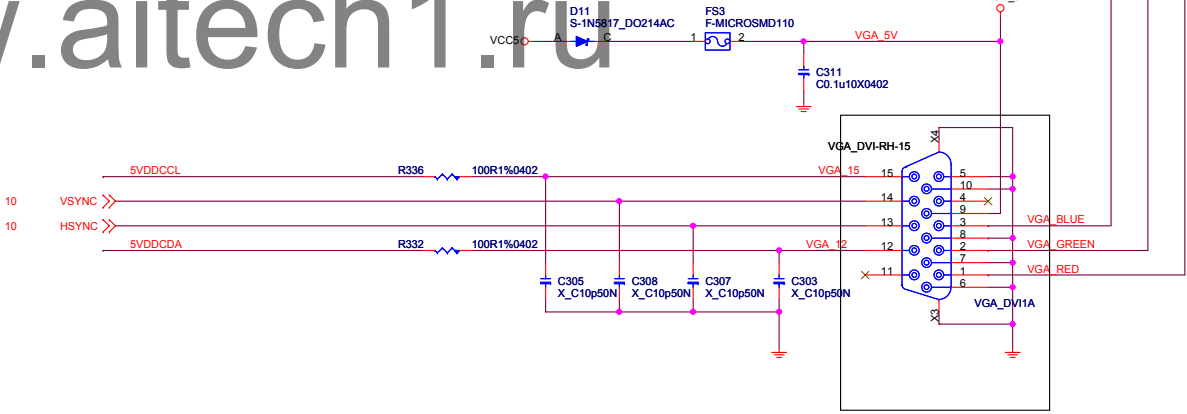
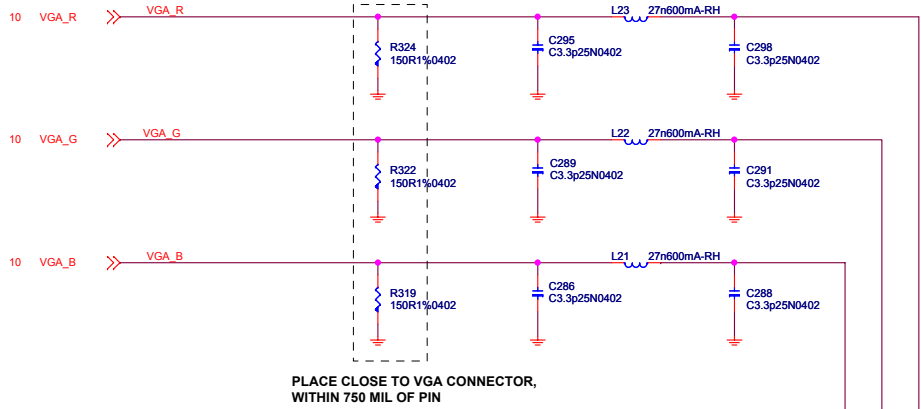
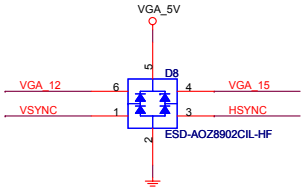
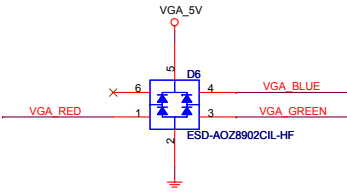
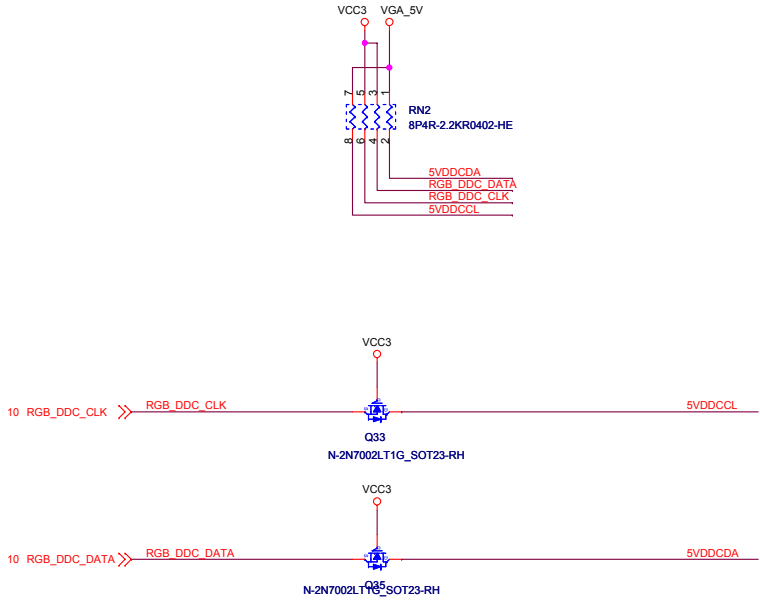
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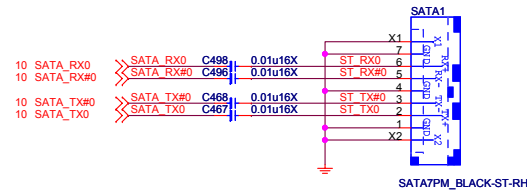
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Levelshift

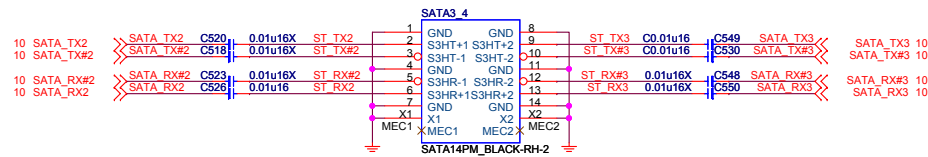


### SATA 6G PORT 0,1

3.0 white

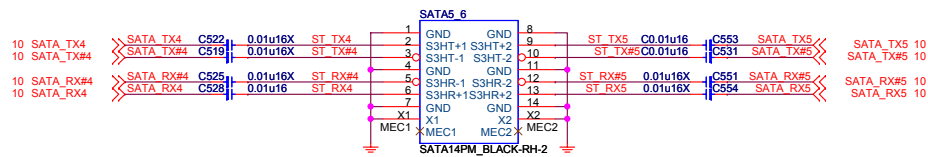


### SATA 6G PORT 2,3



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### SATA 6G PORT 4,5

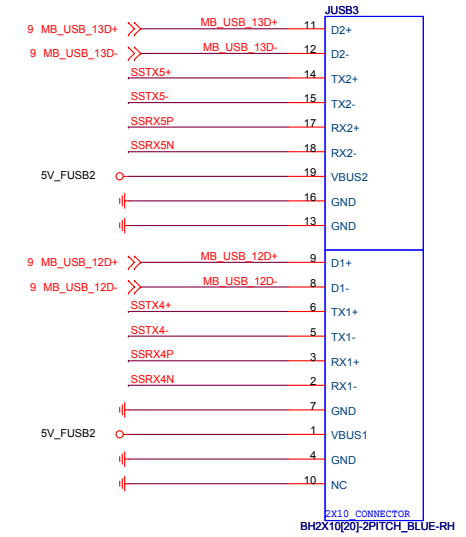
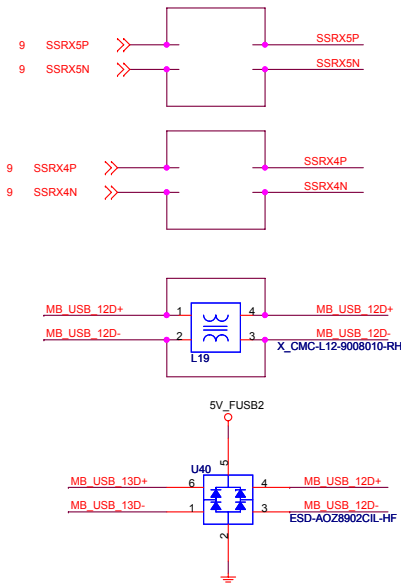
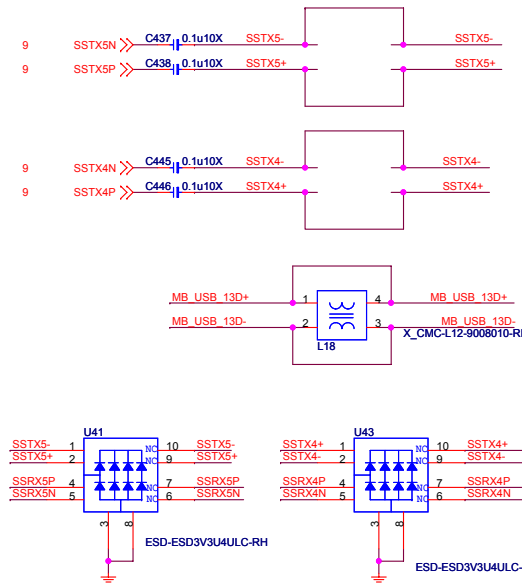
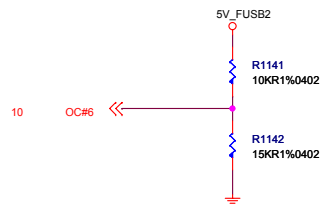


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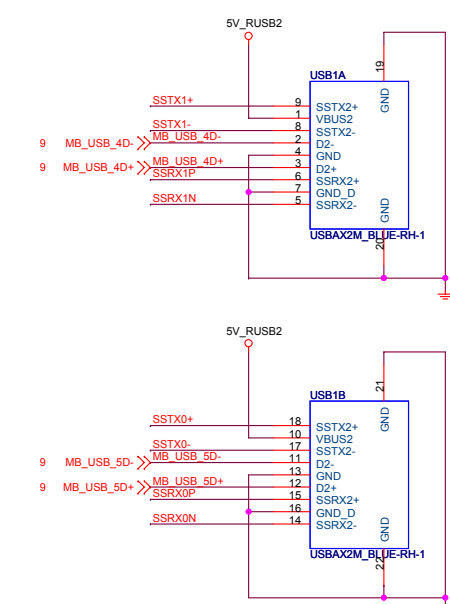
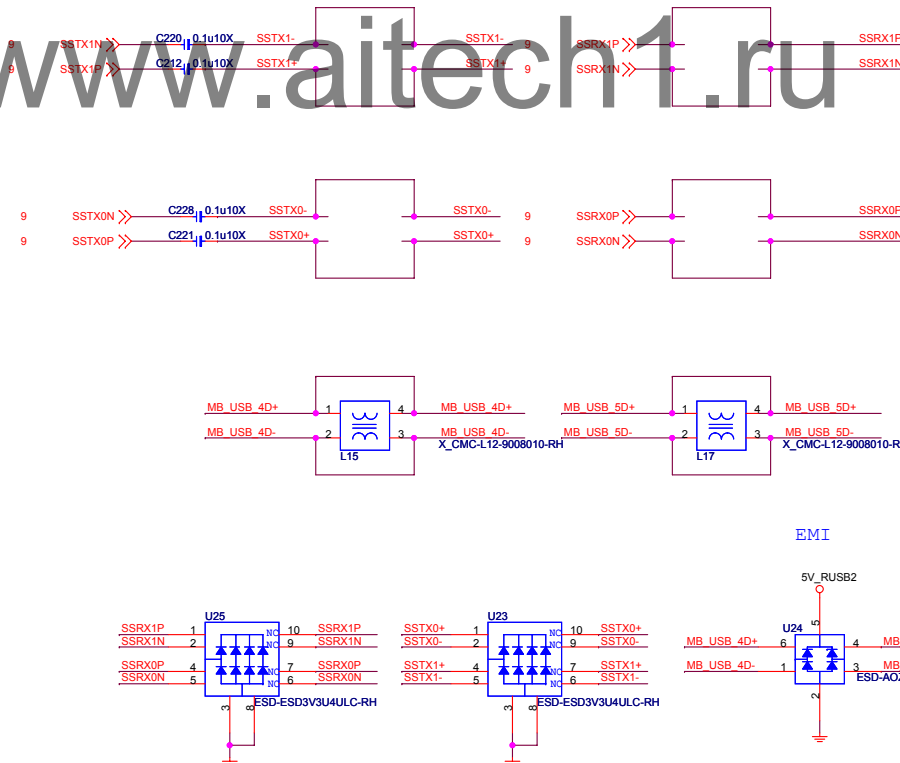
MS-7758

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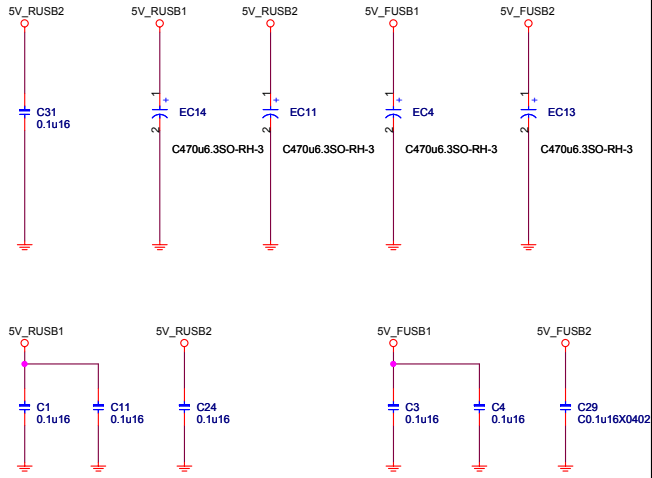
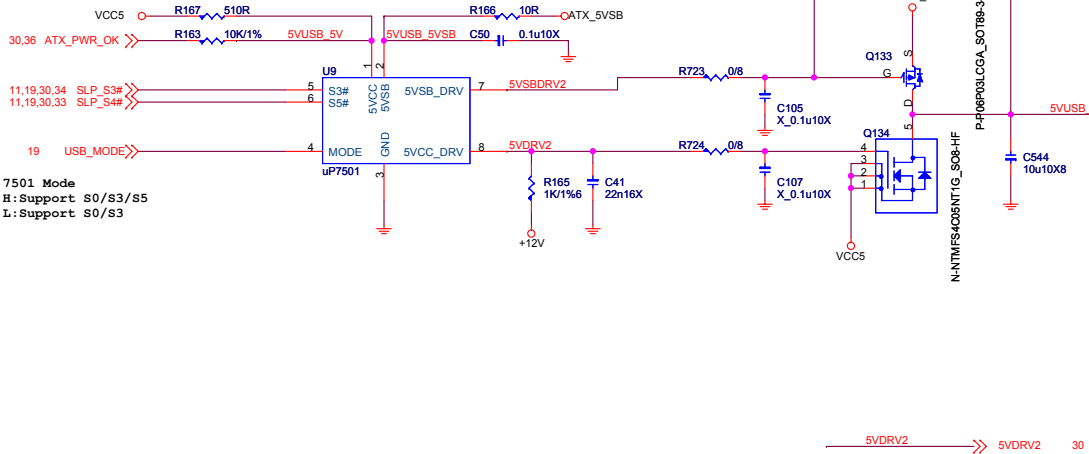




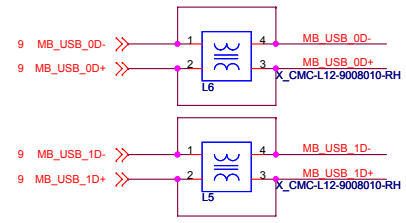
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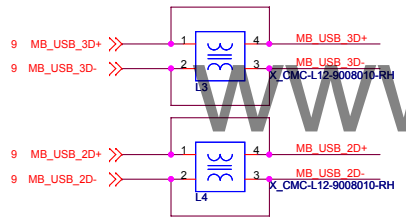
USB2.0/PS2 POWER Control  
**5VDIMM FOR DDR**



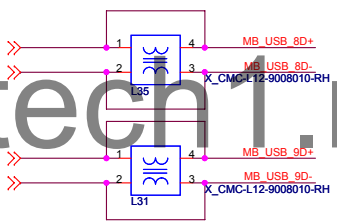
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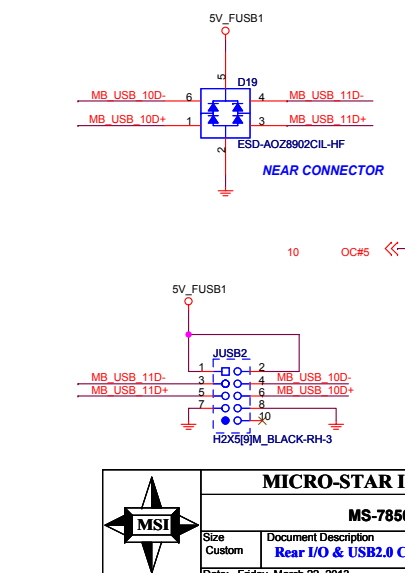
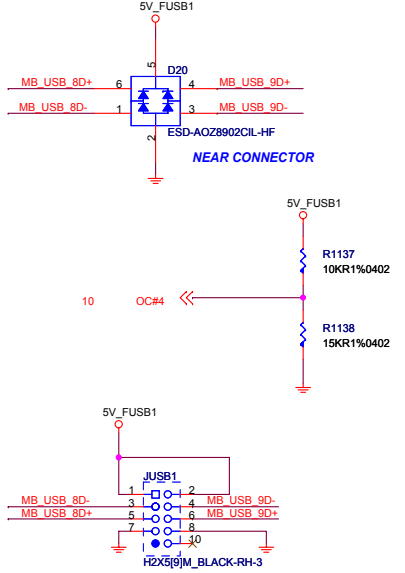
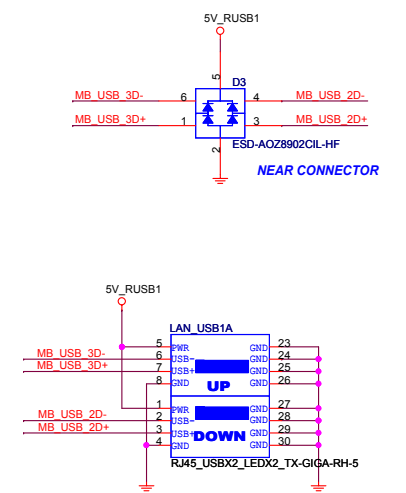
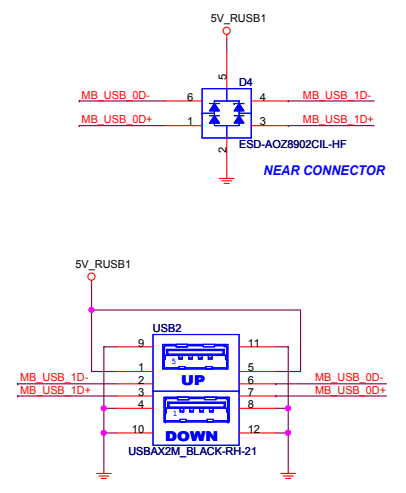
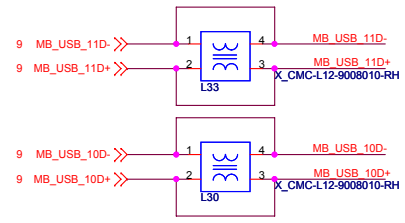
**FRONT USB PORT4,5(With Lan)**




**FRONT USB PORT8,9**



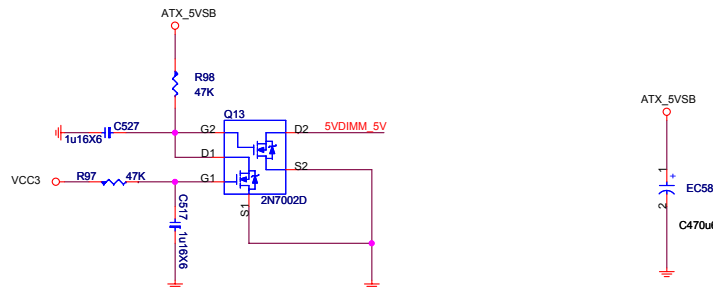
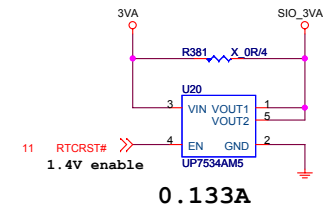
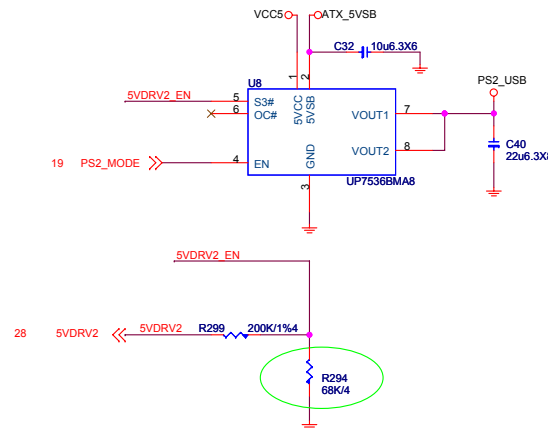
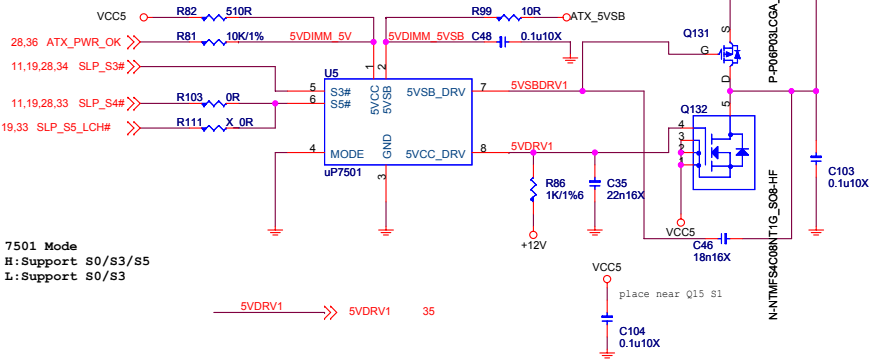
**FRONT USB PORT 10,11**



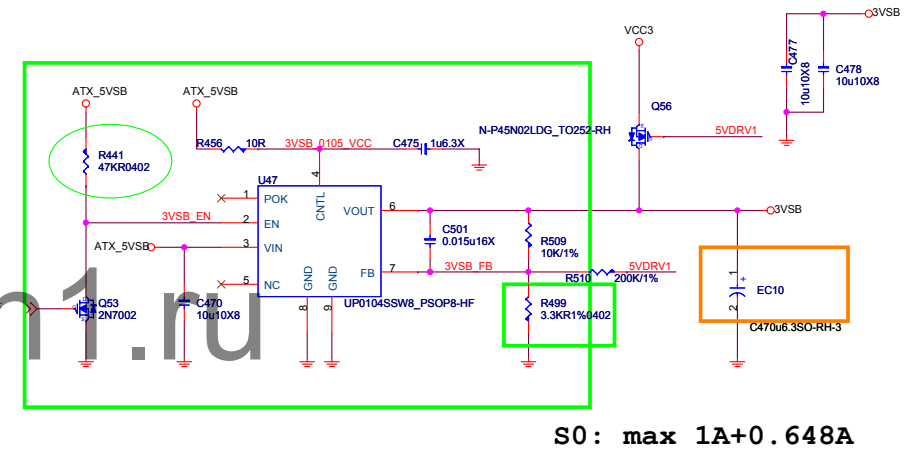
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## 5VDIMM FOR DDR

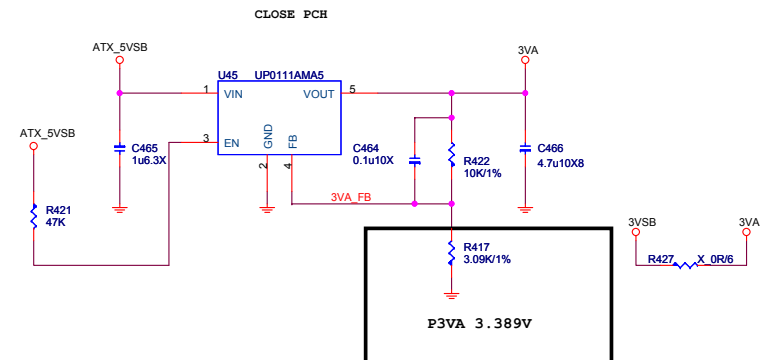


## 3VSB



## 3VA

20mA

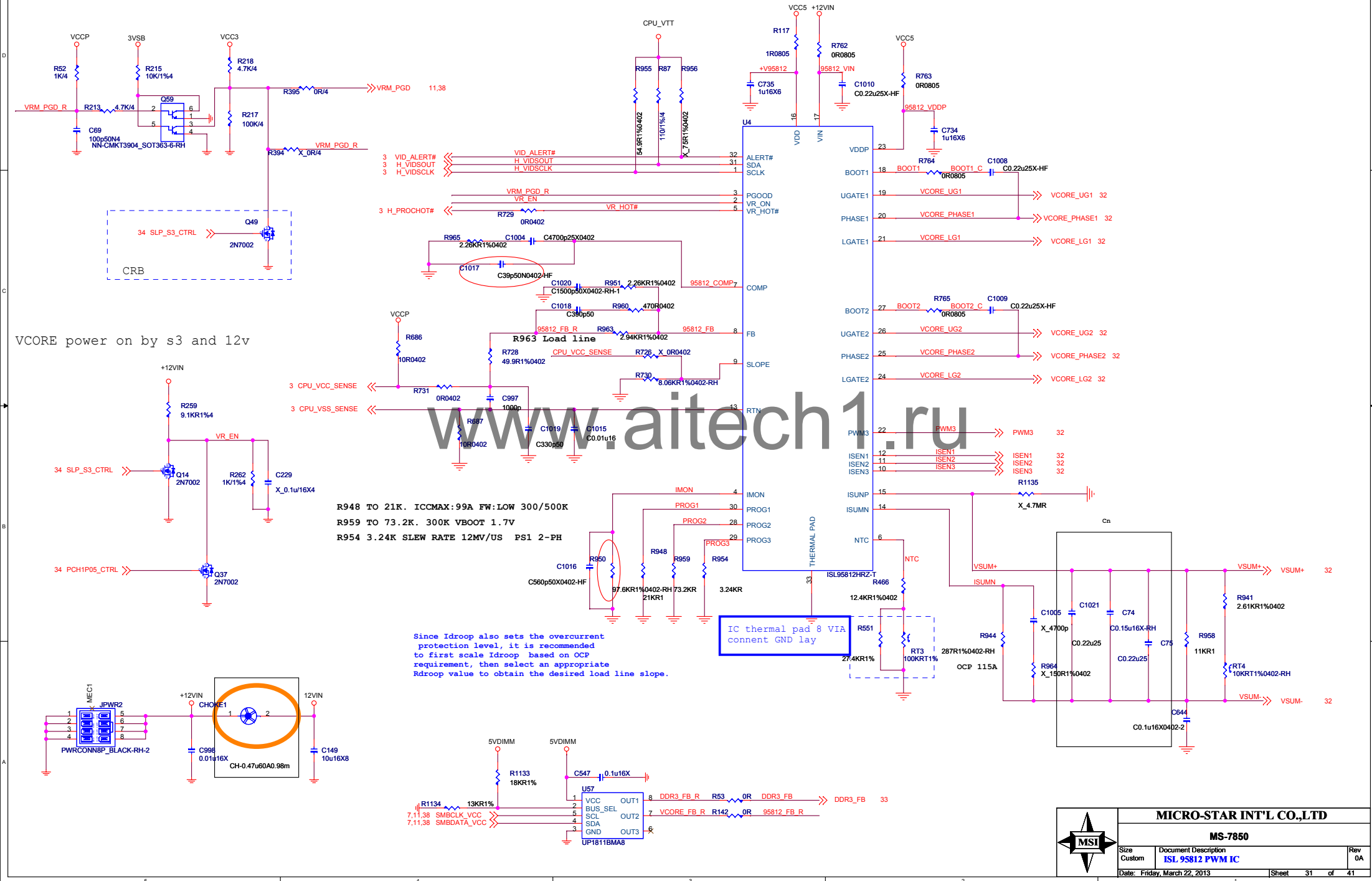


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ISL95812 FOR VR12.5 suggest  
schematic

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## DDR Power:1.5V

DDR3\_1.5V ICCMAX 24A

4.5A FOR CPU

12A FOR 4DIMM

1.1A FOR DDR VTT

6A FOR DDR PCH

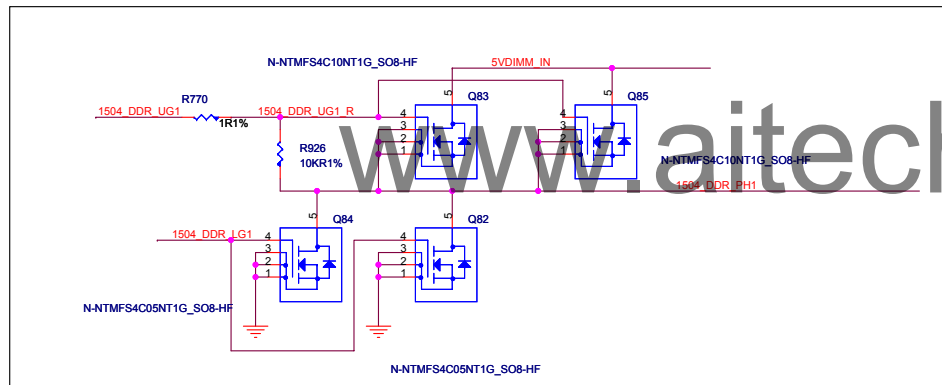
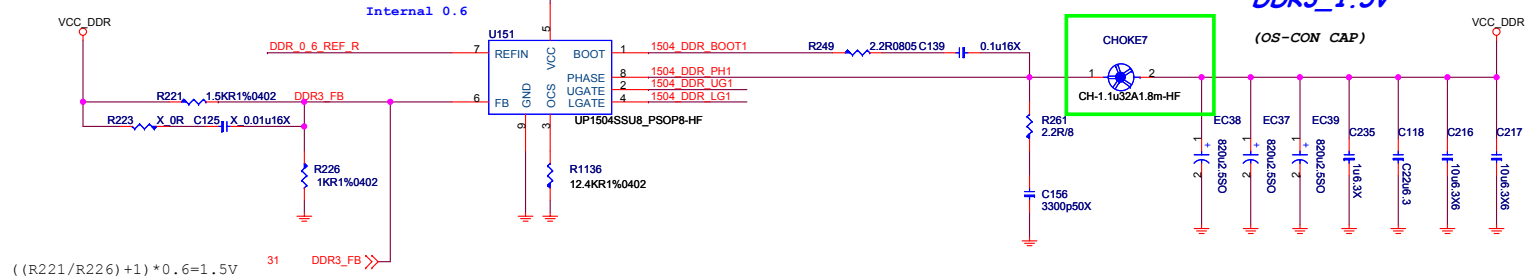
Tripple=9.6

$4.7 * 2 * 1 = 9.4A < 9.6A$

OCP  $24 * 1.5 = 36A$

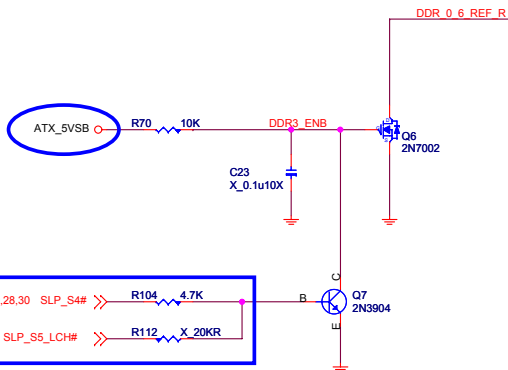
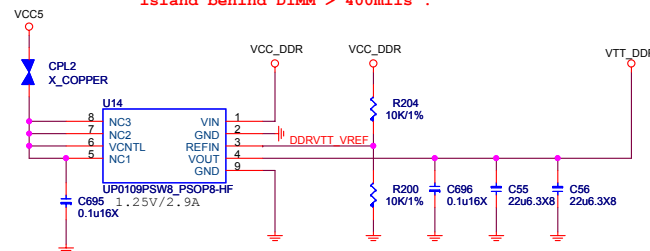
$36A = 20\mu A * R_{ocs} / 4 * R_{dson}$  (Low side 1.7mohm)

$R_{ocs} = 12.4K \text{ ohm}$



## DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



P.S. Only for meet Intel power down sequence.

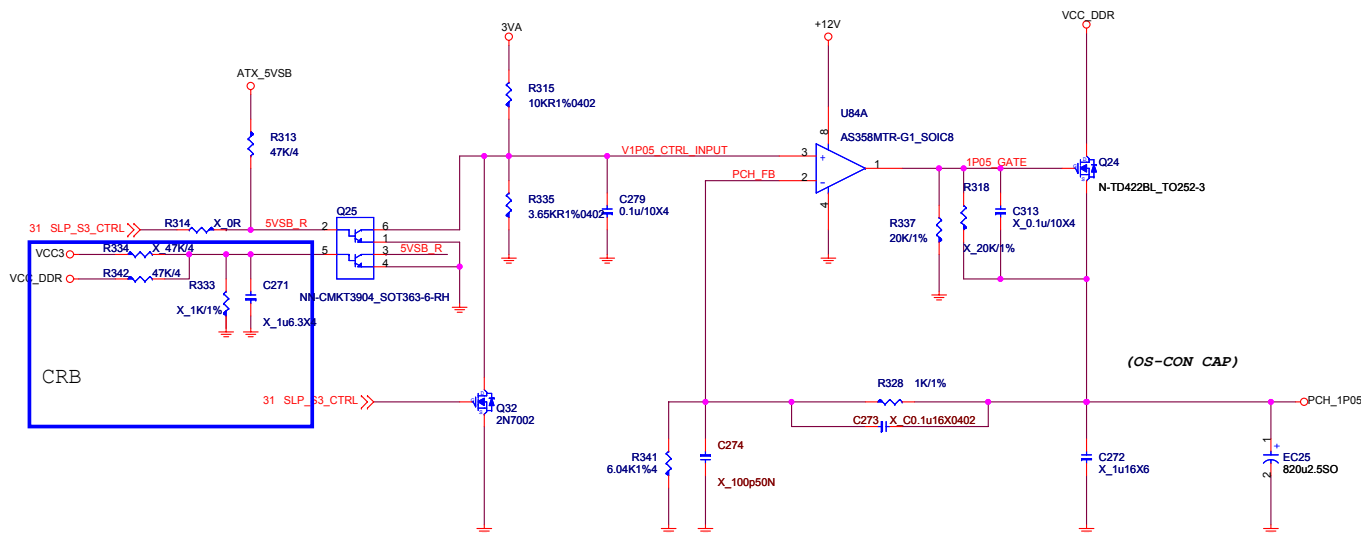


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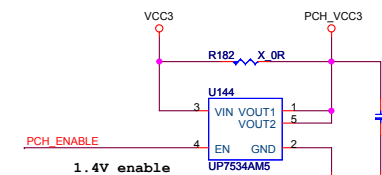
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Custom	DDR Power-UP1513 UP1504S	0A
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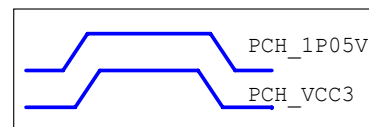
**PCH Power:1.05V 5.747A**



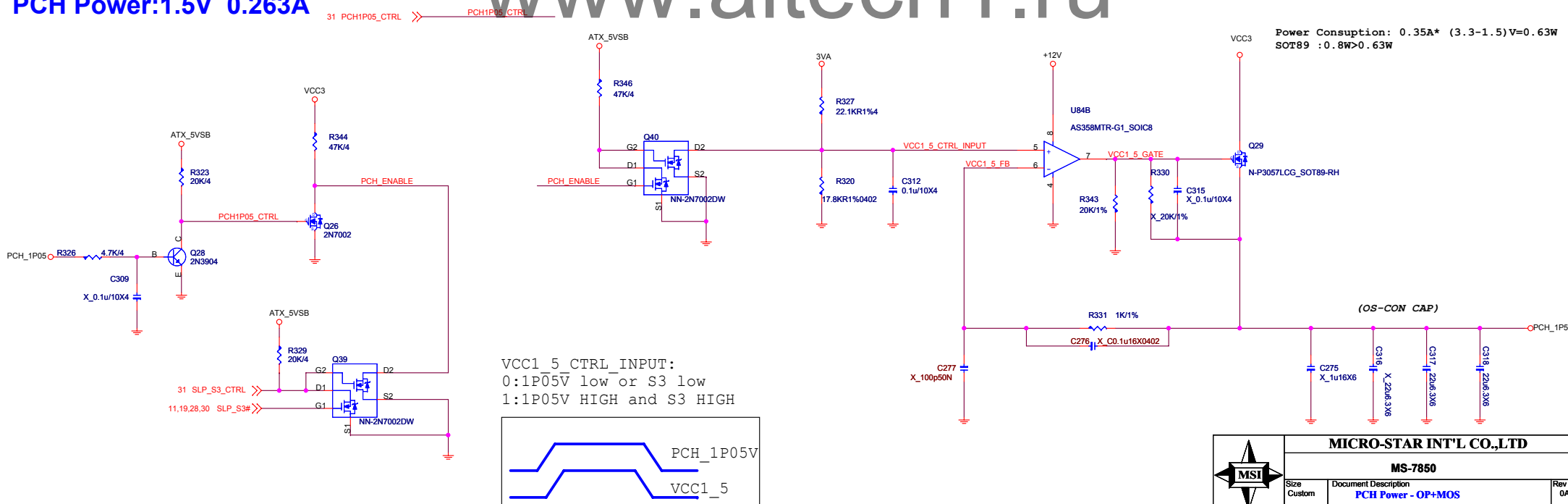
0.133A



```
VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH
```



**PCH Power:1.5V 0.263A**

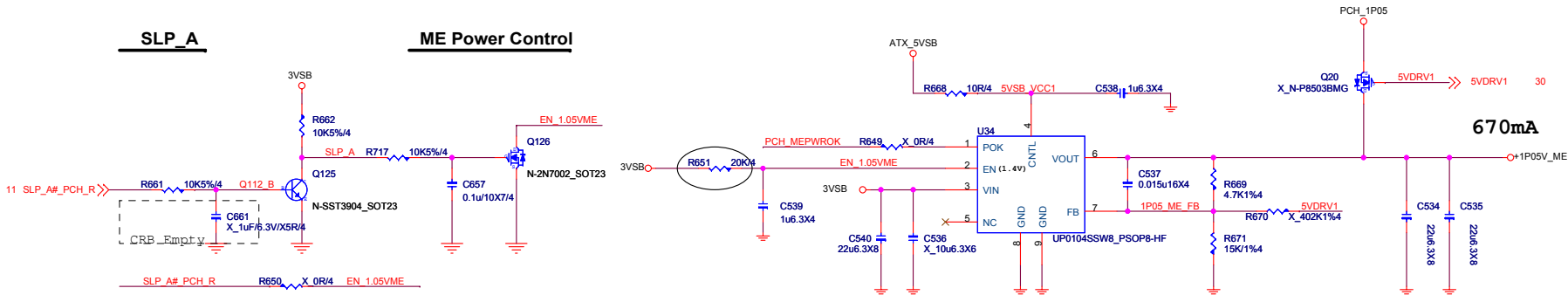


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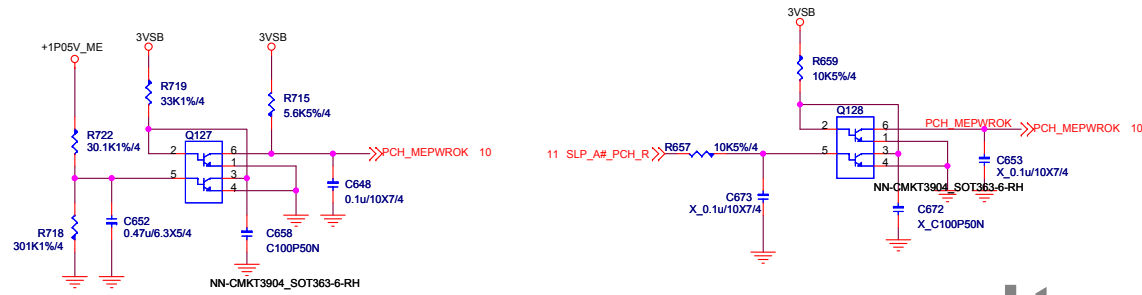
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Size Custom	Document Description <b>PCH Power - OP+MOS</b>	Rev 0A
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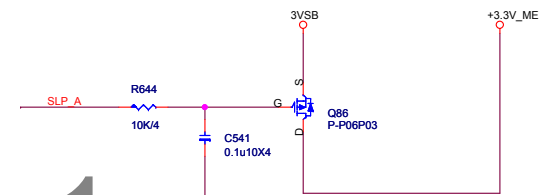
**+1.05V\_ME(VCCIO\_ME)**



**PCH\_MEPWROK**



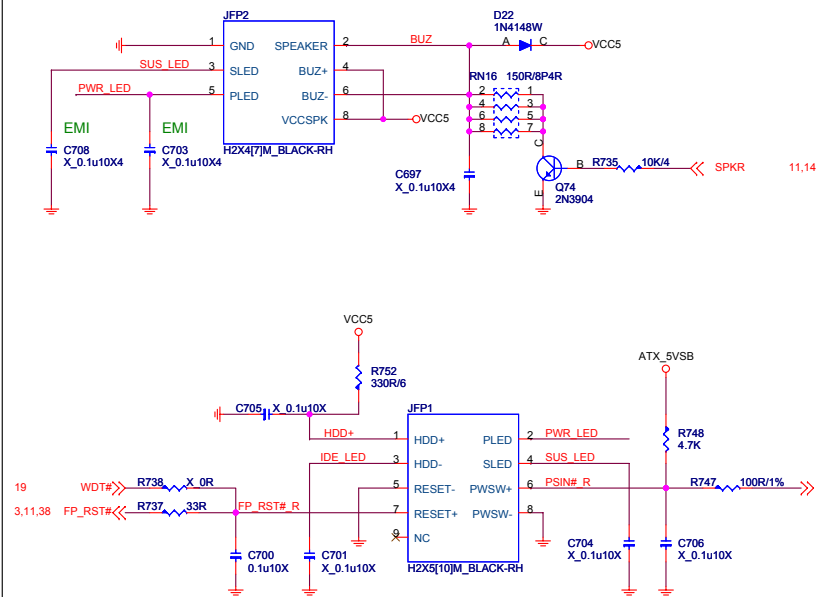
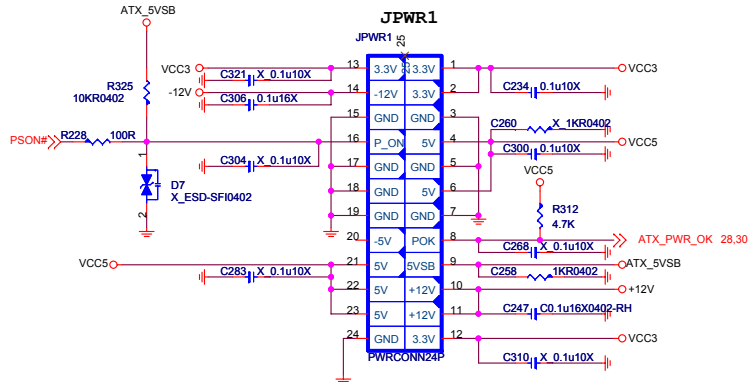
**+3.3V\_ME**



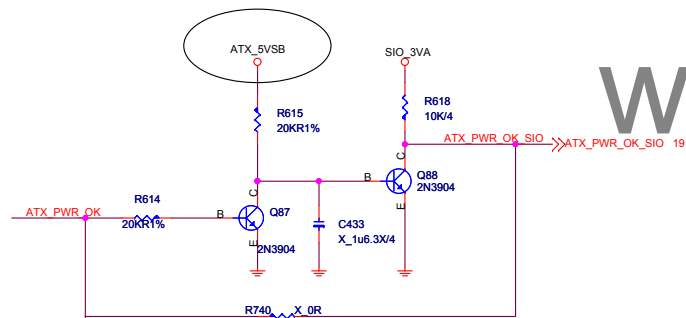
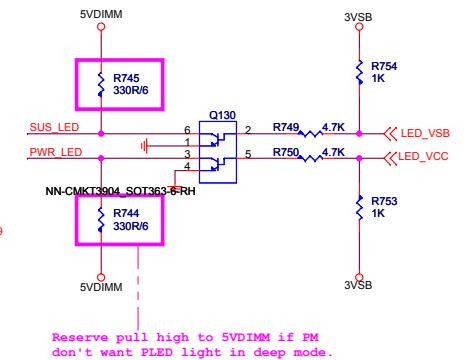
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Title				Size				Document Number				Rev			
<Title>												<Rev Code>			
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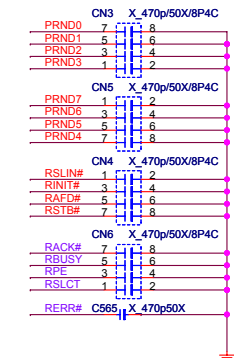
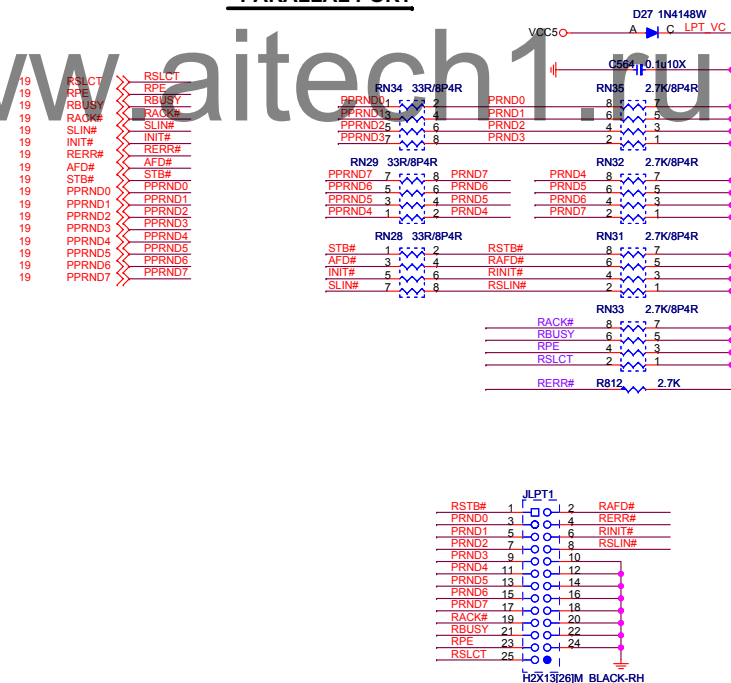
## ATX POWER CONNECTOR



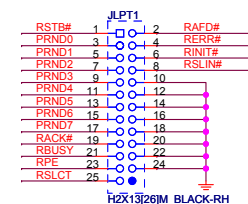
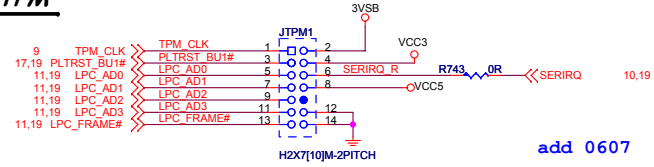
**LED ( for Fintek 71869)**



## PARALLAL PORT



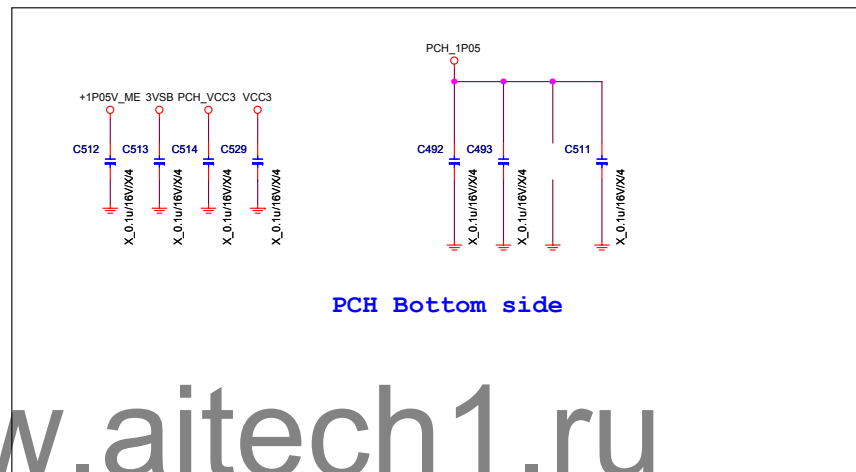
**TPM**



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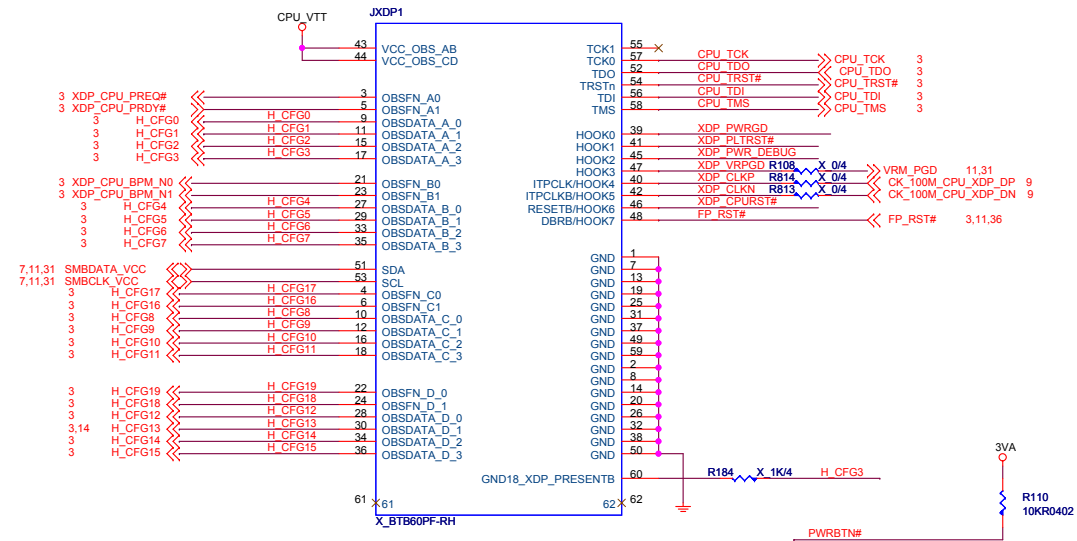


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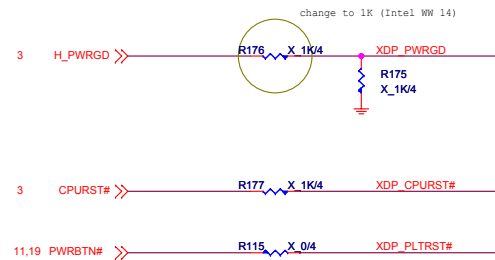
**Reserve debug port 5020**



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3 PWR\_DEBUG X 04 XDP\_PWR\_DEBUG CPU\_TDO R815 S14 PCH\_1P05

PLACE NEAR XDP CONNECTOR



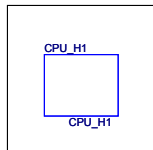
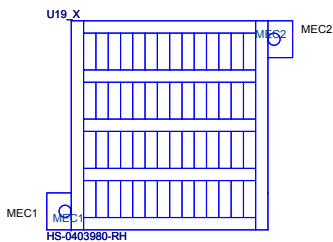
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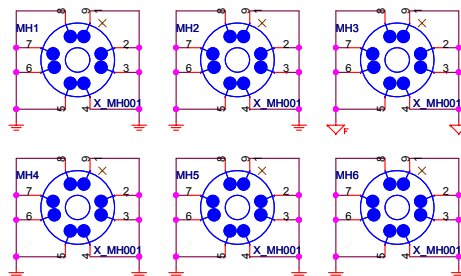
Size Custom	Document Description <b>JXDP</b>	Rev 0A
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5 4 3 2 1

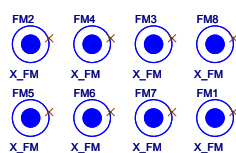
Voltage test point



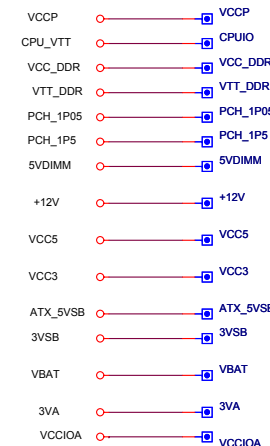
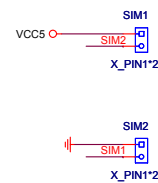
Mounting Holes



Optical Fiducial Marks-120



Simulation



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